

## 4Gb Built-in ECC DDR3/DDR3L SDRAM Specification

### Specifications

- Density: 4G bits
- Organization
  - 8 banks x 64M words x 8 bits
  - 8 banks x 32M words x 16 bits
- Package
  - 78-ball FBGA
  - 96-ball FBGA
- Power supply:
  - HP, -GM, -DK
  - VDD, VDDQ = 1.35 V (1.283 to 1.45 V)
  - Backward compatible with DDR3 operation  
VDD, VDDQ = 1.5 V (1.425 to 1.575 V)
- Data Rate: 1866 Mbps (max.)
- 1KB page size (x8)
  - Row address: AX0 to AX15
  - Column address: AY0 to AY9
- 2KB page size (x16)
  - Row address: AX0 to AX14
  - Column address: AY0 to AY9
- Eight internal banks for concurrent operation
- Burst lengths(BL): 8 and 4 with Burst Chop(BC)
  - Use burst length of 8 for data consistency with ECC
- Burst type(BT)
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11, 13, 14
- CAS Write Latency (CWL): 5, 6, 7, 8, 9, 10
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh: auto-refresh, self-refresh
- Average refresh period
  - 7.8 us at TC ≤ +85°C
  - 3.9 us at TC > +85°C
- Operating temperature range
  - TC = 0°C to +95°C (Commercial grade)
  - TC = -40°C to +95°C (Industrial grade)
  - TC = -40°C to +105°C (Automotive grade 2)
  - TC = -40°C to +125°C (Automotive grade 1)

### Features

- Built-in ECC (Error Correcting Code)
  - Single bit error correction and double bit error detection in 64bit data
  - /DED (Double bit Error Detection) pin sends a fault detection signal to notify SoC of memory data error state when uncorrectable error is found in DRAM\*
  - Compatible with conventional JEDEC standard DRAM; /DED pin is connected or unconnected does not affect ECC function; /DED pin state or level does not affect ECC function
  - Use Burst Chop and Data Mask may restrict the ECC functionality
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Double data-rate architecture: two data transfers per clock cycle
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for Power-up sequence and reset function
- SRT(Self Refresh Temperature) range:
  - Normal/Extended
- Auto Self-Refresh (ASR)
- Programmable output driver impedance control
- JEDEC compliant DDR3/DDR3L
- Row-Hammer-Free (RH-Free): detection/blocking circuit inside

Note: /DED pin should be terminated at the VTDD and will be output low level when DED occurs.

### Key Timing Parameters

Speed Grade	Data Rate(Mbps)	CL	nRCD	nRP
-HP <sup>1, 2</sup>	1866	13	13	13
-GM <sup>1</sup>	1600	11	11	11
-DK	1333	9	9	9

Notes:

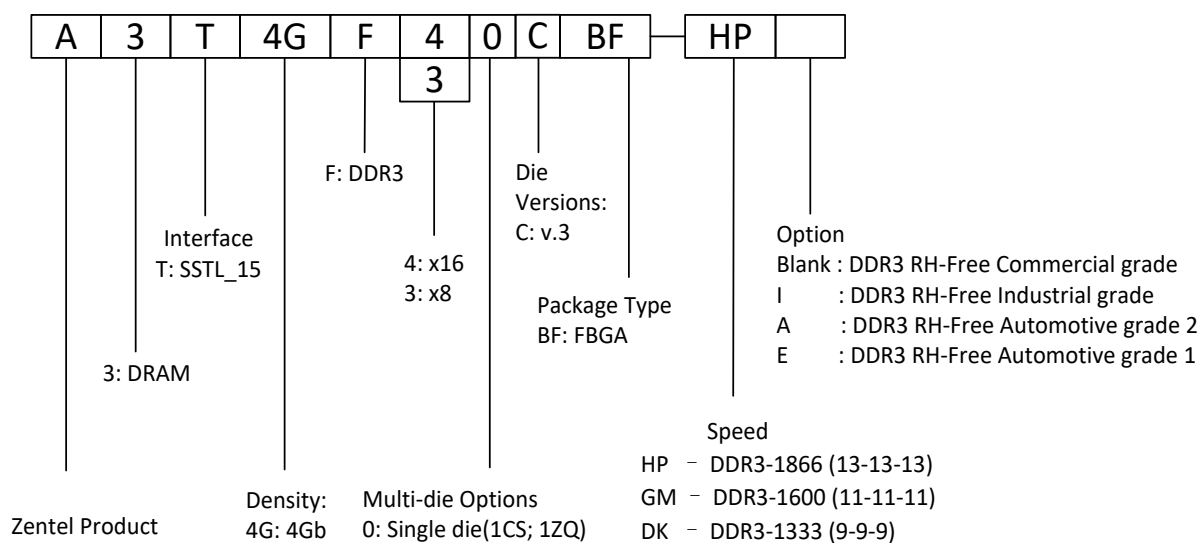
1. Backward compatible to 1333, CL-nRCD-nRP = 9-9-9
2. Backward compatible to 1600, CL-nRCD-nRP = 11-11-11

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## 1. Ordering Information

Part Number	Organization (words x bits)	Internal Banks	Speed bin (CL-nRCD-nRP)	Package	RH-Free		
A3T4GF30CBF-HP/-HPI/-HPA/-HPE	512M × 8	8	DDR3/DDR3L -1866 (13-13-13)	78-ball FBGA	Yes		
A3T4GF30CBF-GM/-GMI/-GMA/-GME			DDR3/DDR3L -1600 (11-11-11)				
A3T4GF30CBF-DK/-DKI/-DKA/-DKE			DDR3/DDR3L -1333 (9-9-9)				
A3T4GF40CBF-HP/-HPI/-HPA/-HPE	256M × 16		DDR3/DDR3L -1866 (13-13-13)	96-ball FBGA			
A3T4GF40CBF-GM/-GMI/-GMA/-GME			DDR3/DDR3L -1600 (11-11-11)				
A3T4GF40CBF-DK/-DKI/-DKA/-DKE			DDR3/DDR3L -1333 (9-9-9)				



## 2. Built-in ECC Function and its Advantages

### 2.1. Built-in ECC Function

The built-in ECC detects and corrects bit errors. When 64bit data (8-DQ, 8-Burst) come to write data area, 8bit parity for SEC (single bit error correction)/DED ECC will be generated from the 64bit data by the built-in ECC module. The 64bit write data will write to normal memory array. 8 bit parity data will write to ECC memory array. When later carrying out a Read command for that location, the built-in ECC module analyzes and compares the data from normal memory array and the parity data from ECC memory array to detect and correct the bit error. If the ECC built-in module cannot correct all the bits during the Read burst (more than one-bit error per 64bit of the stored data), the built-in ECC module notifies SoC of a fault detection signal "low level" through /DED pin. The /DED pin is an open-drain output.

To reset the output of DED, perform the initialization operation or EXIT of MPR.

### 2.2. Built-in ECC Advantages

#### Reduce system failure rate

- Each Built-in ECC DDR has low failure rate
- DRAM failure prediction is possible

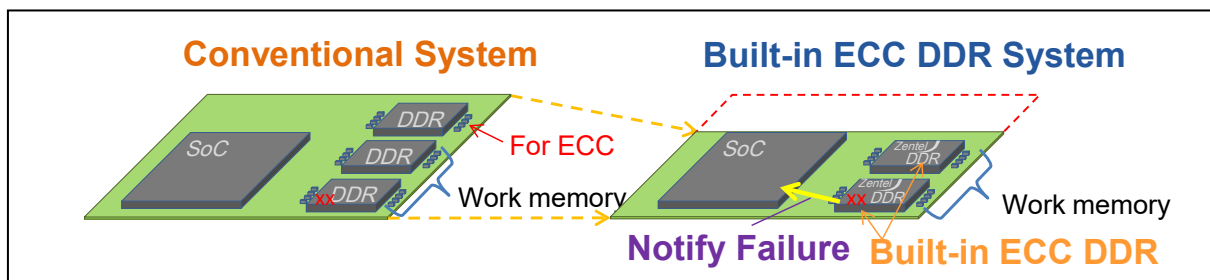
#### Reduce power consumption and EMI noise

- Less current consumption when ECC implemented in DRAM than when implemented in SoC
- Reduce system circuit complexity and the number of DDR used for ECC

#### Reduce system cost

- Reduce the number of DDR, resistor, capacitor for ECC and board area

A system configuration example is shown below:





### 3. Package Ball Assignment

78-ball, FBGA (x8 organizations)							96 ball, FBGA (x16 organizations)						
	1	2	3	7	8	9		1	2	3	7	8	9
A	VSS	VDD	NC	NU(/TDQS)	VSS	VDD	A	VDDQ	DQ13	DQ15	DQ12	VDDQ	VSS
B	VSS	VSSQ	DQ0	DM/TDQS	VSSQ	VDDQ	B	VSSQ	VDD	VSS	/DQSU	DQ14	VSSQ
C	VDDQ	DQ2	DQS	DQ1	DQ3	VSSQ	C	VDDQ	DQ11	DQ9	DQSU	DQ10	VDDQ
D	VSSQ	DQ6	/DQS	VDD	VSS	VSSQ	D	VSSQ	VDDQ	DMU	DQ8	VSSQ	VDD
E	VREFDQ	VDDQ	DQ4	DQ7	DQ5	VDDQ	E	VSS	VSSQ	DQ0	DML	VSSQ	VDDQ
F	NC	VSS	/RAS	CK	VSS	/DED	F	VDDQ	DQ2	DQSL	DQ1	DQ3	VSSQ
G	ODT	VDD	/CAS	/CK	VDD	CKE	G	VSSQ	DQ6	/DQSL	VDD	VSS	VSSQ
H	NC	/CS	/WE	A10(AP)	ZQ	NC	H	VREFDQ	VDDQ	DQ4	DQ7	DQ5	VDDQ
J	VSS	BA0	BA2	A15	VREFCA	VSS	J	NC	VSS	/RAS	CK	VSS	/DED
K	VDD	A3	A0	A12(/BC)	BA1	VDD	K	ODT	VDD	/CAS	/CK	VDD	CKE
L	VSS	A5	A2	A1	A4	VSS	L	NC	/CS	/WE	A10(AP)	ZQ	NC
M	VDD	A7	A9	A11	A6	VDD	M	VSS	BA0	BA2	NC	VREFCA	VSS
N	VSS	/RESET	A13	A14	A8	VSS	N	VDD	A3	A0	A12(/BC)	BA1	VDD
							P	VSS	A5	A2	A1	A4	VSS
							R	VDD	A7	A9	A11	A6	VDD
							T	VSS	/RESET	A13	A14	A8	VSS

/xxx indicates active low signal

Pin name	Function	Pin name	Function
A0 to A15 (x8) <sup>*3</sup>	Address inputs	CK, /CK	Differential clock input
A0 to A14 (x16) <sup>*3</sup>	A10(AP):Auto precharge	/CS <sup>*3</sup>	Chip select
	A12(/BC):Burst chop	/RAS, /CAS, /WE <sup>*3</sup>	Command input
BA0 to BA2 <sup>*3</sup>	Bank select	CKE <sup>*3</sup>	Clock enable
ZQ	Reference pin for ZQ calibration	ODT <sup>*3</sup>	ODT control
DQ0 to DQ7 (x8)	Data input/output	/DED	Double bit error detect
DQ0 to DQ15 (x16)		VDD	Supply voltage for internal circuit
DQS, /DQS (x8)	Differential data strobe	VSS	Ground for internal circuit
DQSU, /DQSU, DQSL, /DQSL (x16)		VDDQ	Supply voltage for DQ circuit
DM (x8)	Write data mask	VSSQ	Ground for DQ circuit
DMU, DML (x16)		VREFDQ	Reference voltage for DQ
TDQS, /TDQS (x8)	Termination data strobe	VREFCA	Reference voltage for CA
/RESET <sup>*3</sup>	Active low asynchronous reset	NC <sup>*1</sup>	No connection

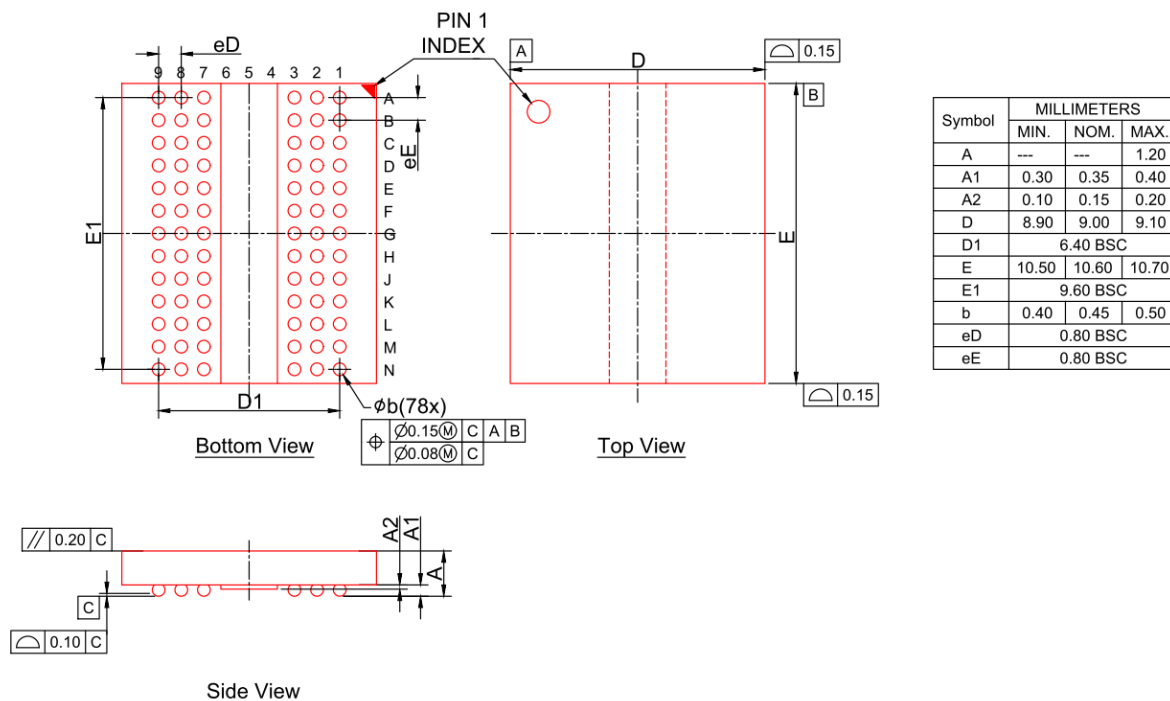
Notes:

- Not internally connected with die
- Don't connect. Internally connected
- Input only pins (address, command, CKE, ODT and /RESET) do not supply termination

## 4. Package Outline Drawing

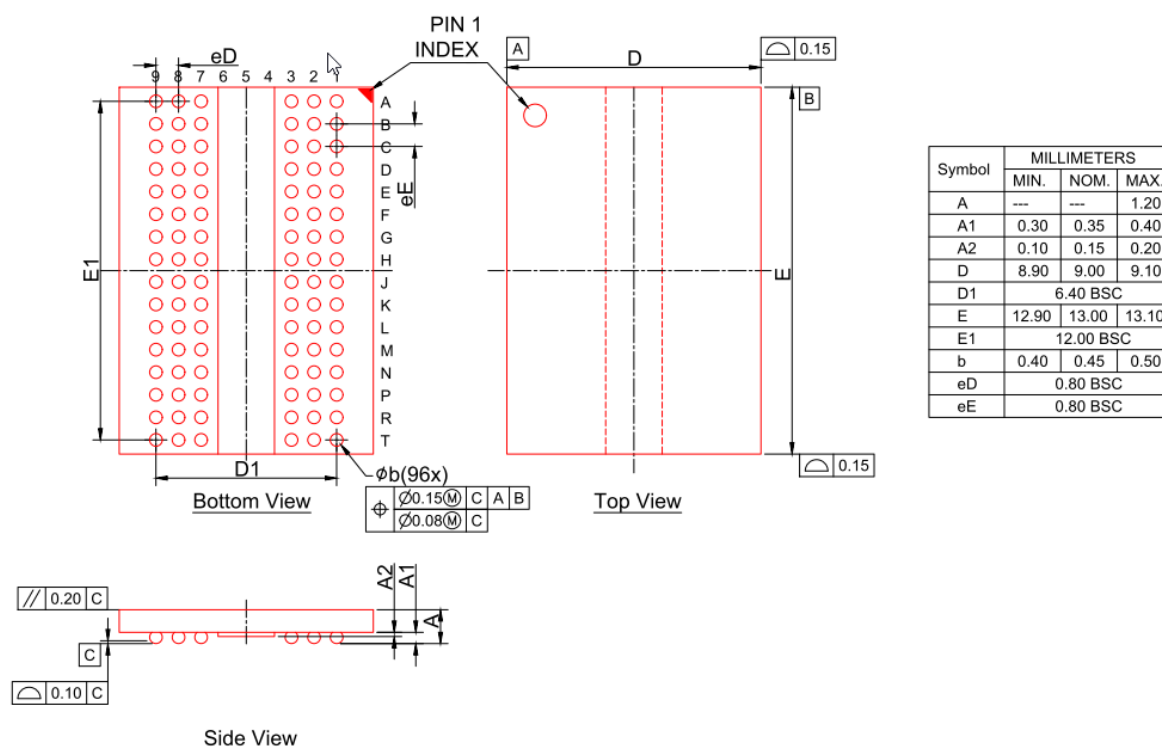
### 78-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)



# 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)



## 5. Electrical Specifications

All voltages are referenced to each VSS (GND)

Execute power-up and Initialization sequence before proper device operation can be achieved.

### 5.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1, 3
Power supply voltage for output	VDDQ	-0.4 to +1.975	V	1, 3
Input voltage	VIN	-0.4 to +1.975	V	1
Output voltage	VOUT	-0.4 to +1.975	V	1
Reference voltage	VREFCA	-0.4 to 0.6 x VDD	V	3
Reference voltage for DQ	VREFDQ	-0.4 to 0.6 x VDDQ	V	3
Termination voltage for /DED	VTTD	-0.4 to +3.6	V	1
Storage temperature	Tstg	-55 to +150	°C	1, 2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

Notes:

- Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- Storage temperature is the case surface temperature on the center/top side of the DRAM.
- VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV

#### Caution:

**Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### 5.2. Operating Temperature Condition

Product grades	Parameter	Symbol	Rating	Unit	Note
Commercial	Operating case temperature	TC	0 to +95	°C	1, 2, 3
Industrial			-40 to +95		
Automotive grade 2			-40 to +105		
Automotive grade 1			-40 to +125		

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C (and +105°C for automotive grade only) case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs
  - If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

### 5.3. Recommended DC Operating Conditions

#### 5.3.1. Recommended DC operating Conditions for DDR3L (1.35V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.283	1.35	1.45	V	1, 2
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1, 2
Termination voltage for /DED	VTTD	1.283	-	2.7	V	2,3

Notes:

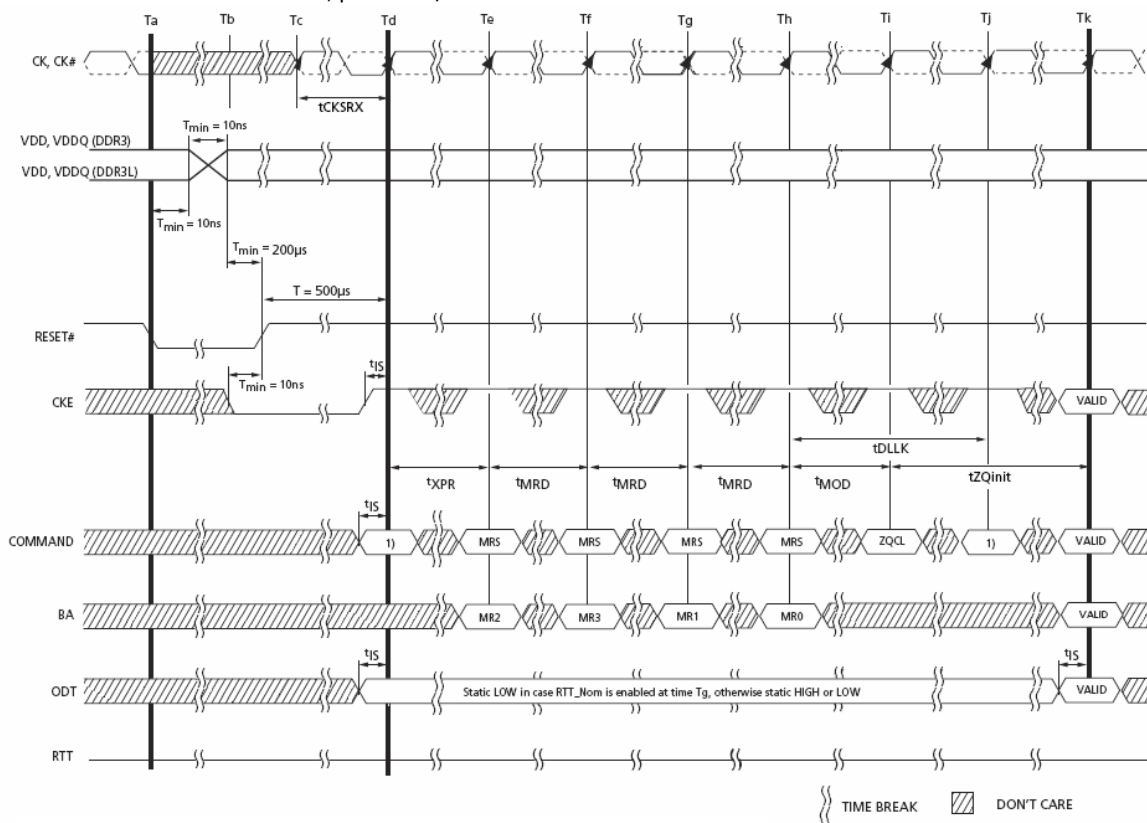
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g. 1sec.)
2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications; Under these supply voltages, the device operates to this DDR3L specification; Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation shown as following timing waveform
3. If you do not use the DED notification, please fix /DED to VSS or OPEN.

#### 5.3.2. Recommended DC operating Conditions for DDR3 (1.5V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2
Termination voltage for /DED	VTTD	1.283	-	2.7	V	3

Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications
2. Under 1.5V operation, the DDR3L device operates to the DDR3 specification under the same speed timings as defined for this device; Once initialized for DDR3 operation, DDR3L operation may only be used if the device in reset while VDD and VDDQ are changed for DDR3L operation shown as below
3. If you do not use the DED notification, please fix /DED to VSS or OPEN.



Notes : From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands

**For DDR3 operation**

**5.4. AC and DC Input Measurement Levels for DDR3**

**5.4.1. AC and DC Input Levels for Single-Ended Command and Address Signals**

Symbol	Parameter	DDR3-1333/1600		DDR3-1866		Unit	Notes
		min	max	min	max		
VIH.CA(DC100)	DC input logic high	VREF + 0.100	VDD	VREF + 0.100	VDD	V	1,5
VIL.CA(DC100)	DC input logic low	VSS	VREF - 0.100	VSS	VREF - 0.100	V	1,6
VIH.CA(AC150)	AC input logic high	VREF + 0.150	Note 2	-	-	V	1, 2, 7
VIL.CA(AC150)	AC input logic low	Note 2	VREF - 0.150	-	-	V	1, 2, 8
VIH.CA(AC135)	AC input logic high			VREF + 0.135	Note 2	V	1, 2, 7
VIL.CA(AC135)	AC input logic low			Note 2	VREF - 0.135	V	1, 2, 8
VIH.CA(AC125)	AC input logic high	-	-	VREF + 0.125	Note 2	V	1, 2, 7
VIL.CA(AC125)	AC input logic low	-	-	Note 2	VREF - 0.125	V	1, 2, 8
VrefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4, 9

**Notes :**

1. For input only pins except RESET#. Vref = VrefCA(DC).
2. See 9.6 "Overshoot and Undershoot Specifications" on page 125.
3. The ac peak noise on Vref may not allow Vref to deviate from VrefCA(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.CA(AC150), VIH.CA(AC135), and VIH.CA(AC125); VIH.CA(AC150) value is used when Vref + 0.150V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is referenced, and VIH.CA(AC125) value is used when Vref + 0.125V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC125); VIL.CA(AC150) value is used when Vref - 0.150V is referenced, VIL.CA(AC135) value is used when Vref - 0.135V is referenced, and VIL.CA(AC125) value is used when Vref - 0.125V is referenced.
9. VrefCA(DC) is measured relative to VDD at the same point in time on the same device

#### 5.4.2. AC and DC Input Levels for Single-Ended Data Signals

Symbol	Parameter	DDR3L-1333/1600		DDR3-1866		Unit	Notes
		min	max	min	max		
VIH.DQ(DC100)	DC input logic high	VREF + 0.100	VDD	VREF + 0.100	VDD	V	1, 5
VIL.DQ(DC100)	DC input logic low	VSS	VREF - 0.100	VSS	VREF - 0.100	V	1, 6
VIH.DQ(AC150)	AC input logic high	VREF + 0.150	Note 2	-	-	V	1, 2, 7
VIL.DQ(AC150)	AC input logic low	Note 2	VREF - 0.150	-	-	V	1, 2, 8
VIH.DQ(AC135)	AC input logic high			VREF + 0.135	Note 2	V	1, 2, 7
VIL.DQ(AC135)	AC input logic low			Note 2	VREF - 0.135	V	1, 2, 8
VIH.DQ(AC125)	AC input logic high	-	-	VREF + 0.125	Note 2	V	1, 2, 7
VIL.DQ(AC125)	AC input logic low	-	-	Note 2	VREF - 0.125	V	1, 2, 8
VRefDQ(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4, 9

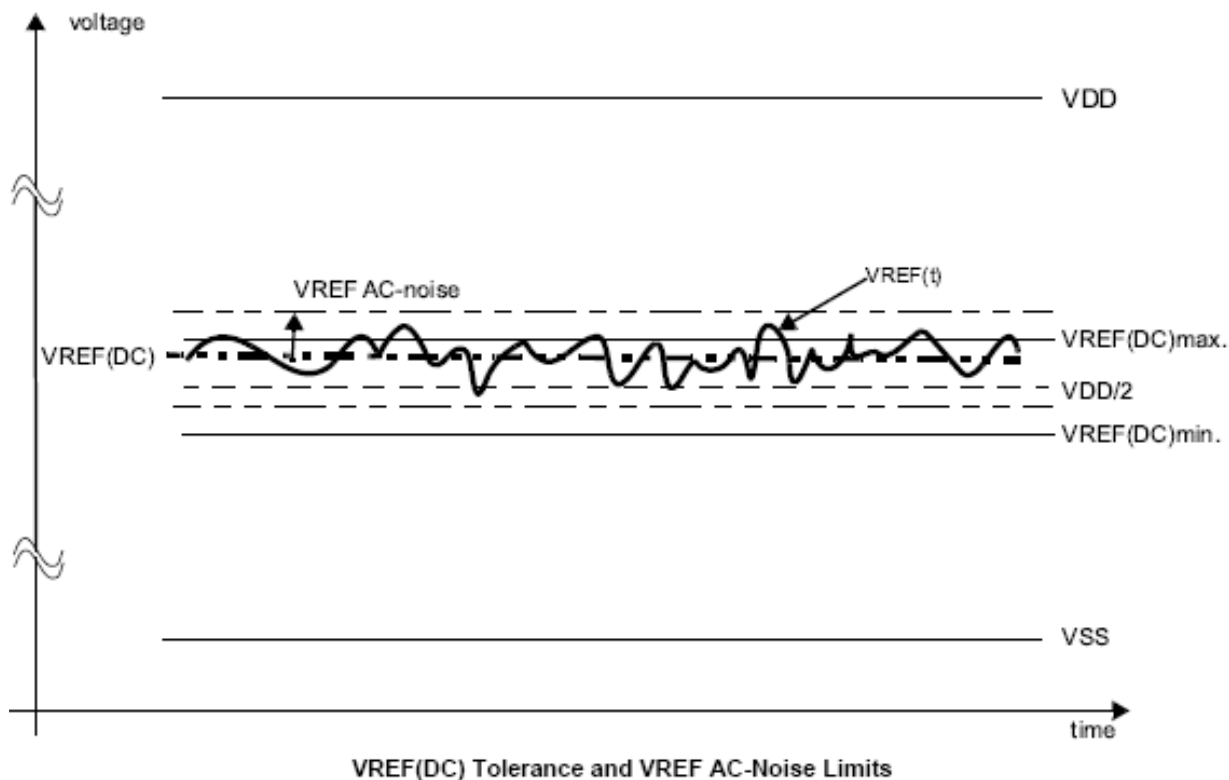
Notes :

1. Vref = VrefDQ(DC).
2. See 9.6 "Overshoot and Undershoot Specifications" on page 125.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)
7. VIH(ac) is used as a simplified symbol for VIH.DQ(AC150), and VIH.DQ(AC135);  
VIH.DQ(AC150) value is used when Vref + 0.150V is referenced, and VIH.DQ(AC135) value is used when Vref + 0.135V is referenced.
8. VIL(ac) is used as a simplified symbol for VIL.DQ(AC150), and VIL.DQ(AC135);  
VIL.DQ(AC150) value is used when Vref - 0.150V is referenced, and VIL.DQ(AC135) value is used when Vref - 0.135V is referenced.
9. VrefDQ(DC) is measured relative to VDD at the same point in time on the same device

### 5.4.3. Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are shown in Figure VREF(DC) Tolerance and VREF AC-Noise Limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in the table of (Single-Ended AC and DC Input Levels for Command and Address). Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than  $\pm 1\%$  VDD.



The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.

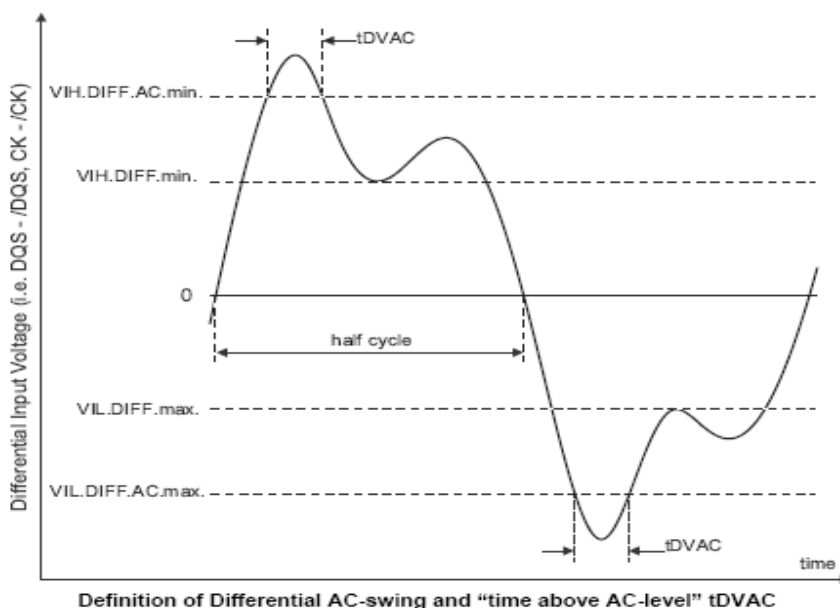
VREF shall be understood as VREF(DC), as defined in figure above, VREF(DC) Tolerance and VREF AC-Noise Limits. This clarifies that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to ac-noise on VREF up to the specified limit ( $\pm 1\%$  of VDD) are included in DRAM timings and their associated deratings.



#### 5.4.4. AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)

##### [Differential AC and DC Input Levels]

Symbol	Parameter	DDR3-1333/1600/1866		Unit	Notes
		min	max		
VIHdiff	Differential input high	+ 0.200	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.200	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
VILdiff(ac)	Differential input low ac	Note 3	2 x (VIL(ac) - Vref)	V	2

NOTE:

- Used to define a differential signal slew-rate.
- For CK - /CK use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - /DQS, DQSL, /DQSL, DQSU, /DQSU use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined; however, the single-ended signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

##### [Allowed time before ringback (tDVAC) for CK - /CK and DQS - /DQS]

Slew Rate [V/ns]	DDR3-1333/1600				DDR3-1866	
	tDVAC [ps] @ [VIH/Ldiff(AC)] = 350mV		tDVAC [ps] @ [VIH/Ldiff(AC)] = 300mV		tDVAC [ps] @ [VIH/Ldiff(AC)] = 300mV	
	min	max	min	max	min	max
> 4.0	75	-	175	-	134	-
4.0	57	-	170	-	134	-
3.0	50	-	167	-	112	-
2.0	38	-	119	-	67	-
1.8	34	-	102	-	52	-
1.6	29	-	81	-	33	-
1.4	22	-	54	-	9	-
1.2	note	-	19	-	note	-
1.0	note	-	note	-	note	-
< 1.0	note	-	note	-	note	-

Note: Rising input differential signal shall become equal to or greater than VIHdiff(AC) level and falling input differential input signal shall become equal to or less than VILdiff(AC) level.

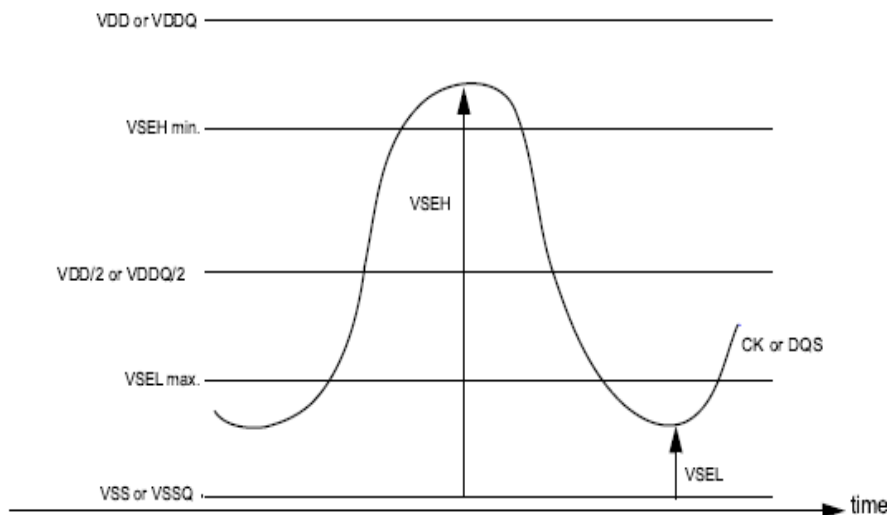
### Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU) has also to comply with certain requirements for single-ended signals.

CK and /CK have to reach VSEH min. / VSEL max. (approximately equal to the AC-levels (VIH(AC) / VIL(AC)) for Address/command signals) in every half-cycle.

DQS, DQSL, DQSU, /DQS, /DQSL, /DQSU have to reach VSEH min./VSEL max. (approximately equal to the AC- levels (VIH(AC) / VIL(AC)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if VIH 150 (AC)/VIL 150 (AC) is used for Address/command signals, then these ac-levels apply also for the single ended components of differential CK and /CK.



Single-Ended Requirement for Differential Signals.

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to  $VDD / 2$ ; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

### [Single-ended levels for CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU]

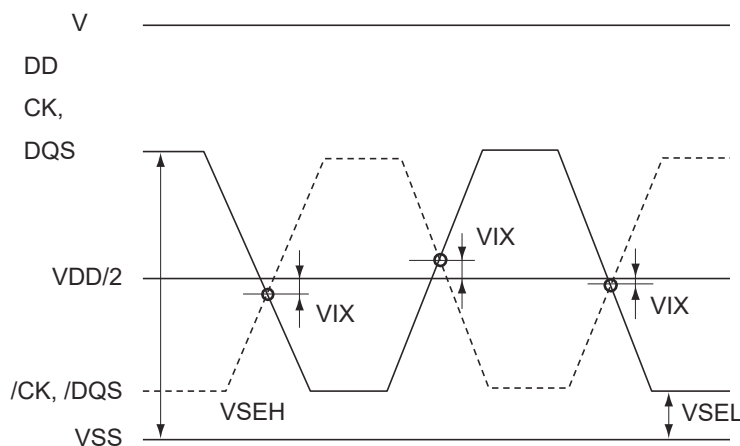
Symbol	Parameter	DDR3-1333/1600/1866		Unit	Notes
		min	max		
VSEH	Single-ended high level for strobes	$(VDD / 2) + 0.175$	Note 3	V	1,2
	Single-ended high level for CK, /CK	$(VDD / 2) + 0.175$	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	$(VDD / 2) - 0.175$	V	1,2
	Single-ended low level for CK, /CK	Note 3	$(VDD / 2) - 0.175$	V	1,2

Notes:

- For CK, /CK use VIH/VIL(AC) of ADD/CMD; for strobes (DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU) use VIH/VIL(AC) of DQs.
- VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single ended components of differential signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot specifications.

#### 5.4.5. Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, /CK and DQS, /DQS) must meet the requirements in table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



**VIX Definition**

[Cross point voltage for differential input signals (CK, DQS)]

Symbol	Parameter	DDR3-1333/1600/1866		Unit	Notes
		min	max		
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV	2
		-175	175	mV	1
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV	2

Notes:

- Extended range for VIX is only allowed for clock and if CK and /CK are monotonic, have a single-ended swing VSEL/VSEH of at least  $VDD/2 \pm 250$  mV, and the differential slew rate of CK - /CK is larger than 3 V/ ns. Refer to the table of Single-ended levels for CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU for VSEL and VSEH standard values.
- The relation between VIX min./max. and VSEL/VSEH should satisfy following.  
 $(VDD/2) + VIX (\text{min.}) - VSEL \geq 25\text{mV}$   
 $VSEH - ((VDD/2) + VIX (\text{max.})) \geq 25\text{mV}$

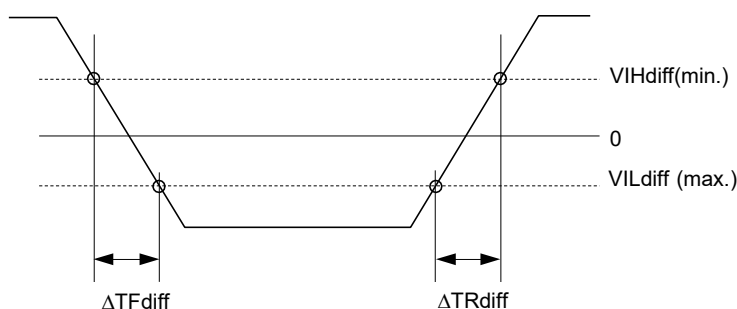
#### 5.4.6. Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as below.

[Differential Input Slew Rate Definition]

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - /CK and DQS - /DQS).	VILdiff(max.)	VIHdiff(min.)	$\frac{VIHdiff(min.) - VILdiff(max.)}{\Delta TRdiff}$
Differential input slew rate for falling edge (CK - /CK and DQS - /DQS).	VIHdiff(min.)	VILdiff(max.)	$\frac{VIHdiff(min.) - VILdiff(max.)}{\Delta TFdiff}$

NOTE: The differential signal (i.e., CK - /CK and DQS - /DQS) must be linear between these thresholds.



$$\text{Falling slew} = \frac{VIHdiff(min.) - VILdiff(max.)}{\Delta TFdiff}$$

$$\text{Rising slew} = \frac{VIHdiff(min.) - VILdiff(max.)}{\Delta TRdiff}$$

**Differential Input Slew Rate Definition for DQS, /DQS and CK, /CK**

## 5.5. AC and DC Output Measurement Levels for DDR3

### 5.5.1. Single Ended AC and DC Output Levels

[Single-ended AC and DC Output Levels]

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
VOH (DC)	DC Output high measurement level (for IV curve linearity)	$0.8 \times VDDQ$	V	
VOM (DC)	DC output middle measurement level (for IV curve linearity)	$0.5 \times VDDQ$	V	
VOL (DC)	DC output low measurement level (for IV curve linearity)	$0.2 \times VDDQ$	V	
VOH (AC)	AC output high measurement level (for output slew rate)	$VTT + 0.1 \times VDDQ$	V	1
VOL (AC)	AC output low measurement level (for output slew rate)	$VTT - 0.1 \times VDDQ$	V	1

NOTE:1. The swing of  $\pm 0.1 \times VDDQ$  is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of  $40 \Omega$  and an effective test load of  $25 \Omega$  to  $VTT = VDDQ/2$ .

### 5.5.2. Differential AC and DC Output Levels

[Differential AC and DC Output Levels]

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output slew rate)	$+0.2 \times VDDQ$	V	1
VOLdiff (AC)	AC differential output low measurement level (for output slew rate)	$-0.2 \times VDDQ$	V	1

NOTE 1. The swing of  $\pm 0.2 \times VDDQ$  is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of  $40 \Omega$  and an effective test load of  $25 \Omega$  to  $VTT = VDDQ/2$  at each of the differential outputs.

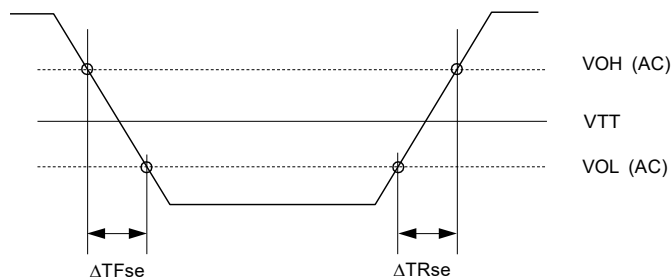
### 5.5.3. Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as below.

#### [Single-ended Output Slew Rate Definition]

Description	Measured		Defined by
	from	to	
Output slew rate for rising edge	VOL (AC)	VOH (AC)	$\frac{VOH (AC) - VOL (AC)}{\Delta TRse}$
Output slew rate for falling edge	VOH (AC)	VOL (AC)	$\frac{VOH (AC) - VOL (AC)}{\Delta TFse}$

NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.



$$\text{Falling slew} = \frac{VOH (AC) - VOL (AC)}{\Delta TFse}$$

$$\text{Rising slew} = \frac{VOH (AC) - VOL (AC)}{\Delta TRse}$$

#### Output Slew Rate Definition for Single-Ended Signals

#### [Output Slew Rate (Single-ended)]

Parameter	Symbol	Speed	min.	max.	Unit
Single-ended Output Slew Rate	SRQse	DDR3-1866	2.5	5	V/ns
		DDR3-1600	2.5	5	
		DDR3-1333	2.5	5	

Remark: SR = slew rate. se = single-ended signals. Q = Query output

Note: 1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

- is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
- is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5V/ns applies.

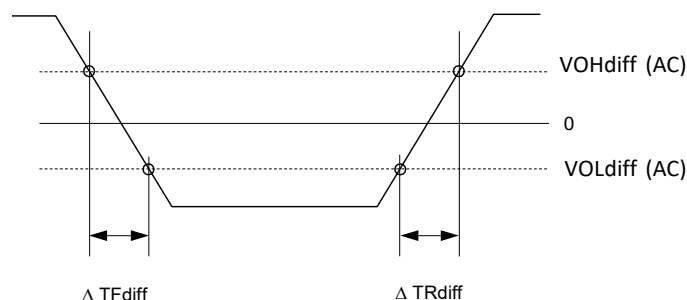
#### 5.5.4. Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as below.

##### [Differential Output Slew Rate Definition]

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff (AC)	VOHdiff (AC)	$\frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TRdiff}$
Differential output slew rate for falling edge	VOHdiff (AC)	VOLdiff (AC)	$\frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TFdiff}$

NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.



$$\text{Falling slew} = \frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TFdiff}$$

$$\text{Rising slew} = \frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TRdiff}$$

#### Differential Output Slew Rate Definition

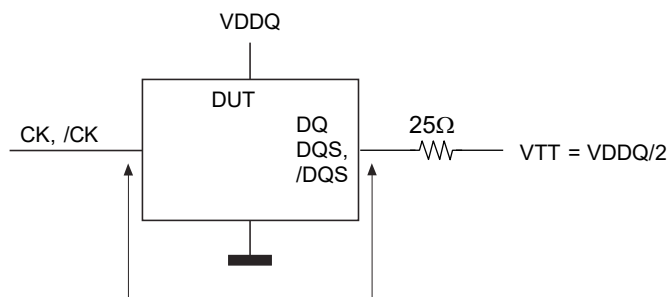
##### [Differential Output Slew Rate]

Parameter	Symbol	Speed	min.	max.	Unit
Differential Output Slew Rate	SRQdiff	DDR3-1866	5	12	V/ns
		DDR3-1600	5	10	
		DDR3-1333	5	10	

Remark: SR = slew rate. diff = differential signals. Q = Query output. For Ron = RZQ/7 setting

#### 5.5.5. Reference Load for AC Timing and Output Slew Rate

This figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.



Reference Output Load

## 5.6. Address / Command /Data Setup, Hold and Derating for DDR3

For all input signals the total tIS, tDS (setup time) and tIH, tDH (hold time) required is calculated by adding the data sheet tIS (base), tDS (base) and tIH (base), tDH (base) value to the  $\Delta tIS$ ,  $\Delta tDS$  and  $\Delta tIH$ ,  $\Delta tDH$  derating value respectively.

Example:  $tDS$  (total setup time) =  $tDS$  (base) +  $\Delta tDS$ .

Setup (tIS, tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF (DC) and the first crossing of VIH (AC) min. Setup (tIS, tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF (DC) and the first crossing of VIL (AC) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF (DC) to AC region', use nominal slew rate for derating value (See the figure of Slew Rate Definition Nominal).

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF (DC) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see the figure of Slew Rate Definition Tangent).

Hold (tIH, tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (DC) max. and the first crossing of VREF (DC). Hold (tIH, tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH (DC) min. and the first crossing of VREF (DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to VREF (DC) region', use nominal slew rate for derating value (See the figure of Slew Rate Definition Nominal).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF (DC) region', the slew rate of a tangent line to the actual signal from the DC level to VREF (DC) level is used for derating value (see the figure of Slew Rate Definition Tangent).

For a valid transition the input signal has to remain above/below VIH/VIL(AC) for some time tVAC (see the table of Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL (AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL (AC).

For slew rates in between the values listed in the tables below, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

### [Address/Command Setup and Hold Base-Values for 1V/ns]

	DDR3-1866	DDR3-1600	DDR3-1333	Unit	Reference
tIS(base) AC175	-	45	65	ps	VIH/VIL(AC)
tIS(base) AC150	-	170	190	ps	VIH/VIL(AC)
tIS(base) AC135	65	-	-	ps	VIH/VIL(AC)
tIS(base) AC125	150	-	-	ps	VIH/VIL(AC)
tIH(base) DC100	100	120	140	ps	VIH/VIL(DC)

Notes:

1. AC/DC referenced for 1V/ns Address/Command slew rate and 2V/ns differential CK, /CK slew rate.
2. The tIS (base) AC150 specifications are adjusted from the tIS(base) AC175 specification by adding an additional 100ps for DDR3-1600/1333 of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV - 150mV) / 1V/ns]
3. The tIS (base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps for DDR3-1866 to accommodate for the lower alternate threshold of 125mV and another 10ps to account for the earlier reference point [(135mV - 125mV) / 1V/ns]



## [Derating values of tIS/tIH AC/DC based AC175 Threshold (DDR-1333, 1066)]

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based AC175 Threshold $\rightarrow VIH(AC) = VREF(DC) + 175\text{ mV}$ , $VIL(AC) = VREF(DC) - 175\text{ mV}$																	
		CK, /CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

## [Derating values of tIS/tIH based-alternate AC150 Threshold (DDR3-1333, 1066)]

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based Alternate AC150 Threshold $\rightarrow VIH(AC) = VREF(DC) + 150\text{ mV}$ , $VIL(AC) = VREF(DC) - 150\text{ mV}$																	
		CK, /CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

## [Derating values of tIS/tIH based-alternate AC135 Threshold (DDR3-1866)]

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based AC135 Threshold $\rightarrow VIH(AC) = VREF(DC) + 135\text{ mV}$ , $VIL(AC) = VREF(DC) - 135\text{ mV}$																	
		CK, /CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$
CMD/ ADD Slew rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

**[Derating values of tIS/tIH based-alternate AC125 Threshold (DDR3-1866)]**

Derating values of $\Delta t_{IH}$ based alternate AC125 threshold (200V - 100V)																	
$\Delta t_{IS}$ , $\Delta t_{IH}$ derating in [ps] AC/DC based AC125 Threshold -> $V_{IH}(AC) = V_{REF}(DC) + 125\text{ mV}$ , $V_{IL}(AC) = V_{REF}(DC) - 125\text{ mV}$																	
		CK, /CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
CMD/ ADD Slew rate V/ns	2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

**[Required time tVAC above VIH(AC) {below VIL(AC)} for valid ADD/CMD transition]**

Slew Rate [V/ns]	DDR3-1066/1333				DDR3-1866			
	tVAC @ AC175 [ps]		tVAC @ AC150 [ps]		tVAC @ AC135 [ps]		tVAC @ AC125 [ps]	
	min	max	min	max	min	max	min	max
> 2.0	75	-	175	-	168	-	173	-
2.0	57	-	170	-	168	-	173	-
1.5	50	-	167	-	145	-	152	-
1.0	38	-	130	-	100	-	110	-
0.9	34	-	113	-	85	-	96	-
0.8	29	-	93	-	66	-	79	-
0.7	22	-	66	-	42	-	56	-
0.6	note	-	30	-	10	-	27	-
0.5	note	-	note	-	note	-	note	-
< 0.5	note	-	note	-	note	-	note	-

Note: Rising input signal shall become equal to or greater than VIH(AC) level and falling input signal shall become equal to or less than VIL(AC) level.

[Data Setup and Hold Base-Values]

Symbol	Reference	DDR3-1866	DDR3-1600	DDR3-1333	Unit	Notes
tDS(base) AC150	VIH/VIL(AC) SR=1V/ns	-	10	30	ps	1
tDS(base) AC135	VIH/VIL(AC) SR=1V/ns	-	40	60	ps	1
tDS(base) AC135	VIH/VIL(AC) SR=2V/ns	68	-	-	ps	2
tDH(base) DC100	VIH/VIL(DC) SR=1V/ns		45	65	ps	1
tDH(base) DC100	VIH/VIL(DC) SR=2V/ns	70	-	-	ps	2

Notes: 1. AC/DC referenced for 1V/ns DQ slew rate and 2V/ns DQS slew rate

2. AC/DC referenced for 2V/ns DQ slew rate and 4V/ns DQS slew rate

[Derating values of tDS/tDH AC/DC based, AC175 (DDR3-1066)]

$\Delta t_{DS}, \Delta t_{DH}$ derating in [ps] AC/DC based AC175 Threshold $\rightarrow$ VIH(AC) = VREF(DC) + 175 mV, VIL(AC) = VREF(DC) - 175 mV																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

[Derating values of tDS/tDH AC/DC based, AC150 (DDR3-1333, 1066)]

$\Delta t_{DS}, \Delta t_{DH}$ derating in [ps] AC/DC based AC150 Threshold $\rightarrow$ VIH(AC) = VREF(DC) + 150 mV, VIL(AC) = VREF(DC) - 150 mV																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$
DQ Slew rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

[Derating values of tDS/tDH AC/DC based, AC135 (DDR3-1333, 1066)]

$\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based Alternate AC135 Threshold -> $V_{IH}(AC) = V_{REF}(DC) + 135\text{ mV}$ , $V_{IL}(AC) = V_{REF}(DC) - 135\text{ mV}$ Alternate DC100 Threshold -> $V_{IH}(DC) = V_{REF}(DC) + 100\text{ mV}$ , $V_{IL}(DC) = V_{REF}(DC) - 100\text{ mV}$																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$
DQ Slew rate V/ns	2.0	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	34	53	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

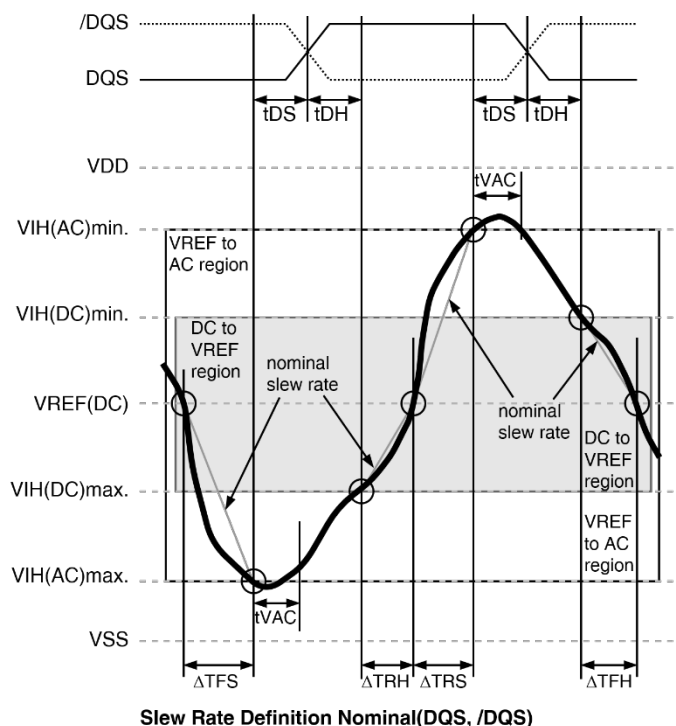
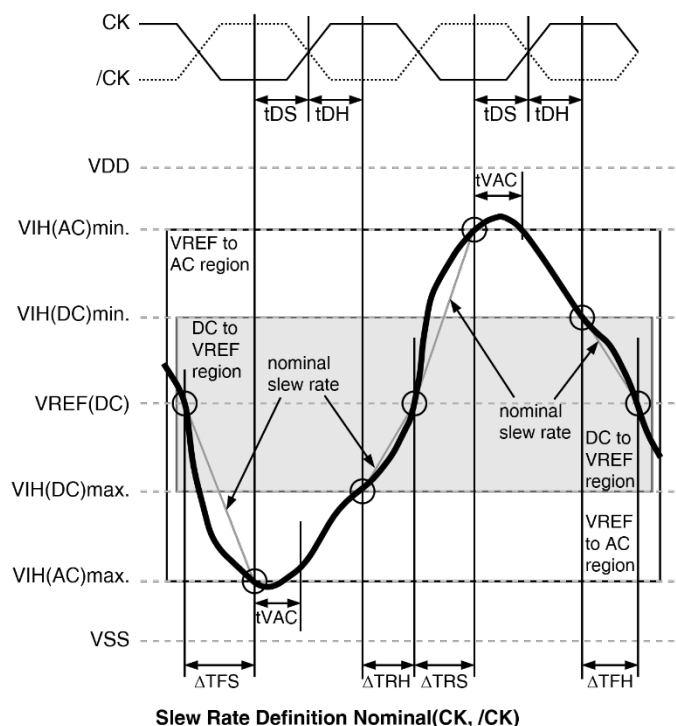
Derating values for DDR3-1866, tDS/tDH (AC135)

Derating Values for: DDR5-1600, tDDR5H (AC100)																									
$\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based																									
Alternate AC135 Threshold -> $V_{IH}(AC) = V_{REF}(DC) + 135\text{ mV}$ , $V_{IL}(AC) = V_{REF}(DC) - 135\text{ mV}$																									
Alternate DC100 Threshold -> $V_{IH}(DC) = V_{REF}(DC) + 100\text{ mV}$ , $V_{IL}(DC) = V_{REF}(DC) - 100\text{ mV}$																									
		DQS, /DQS Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$
DQ Slew rate V/ns	4.0	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-38	-76	-30	-60	

[Required time tVAC above VIH(AC) {below VIL(AC)} for valid DQ transition]

Slew Rate [V/ns]	DDR3-1066 (AC175)		DDR3-1600, 1333, 1066 (AC150)		DDR3-1600, 1333, 1066 (AC135)		DDR3-1866 (AC135)	
	tVAC [ps]		tVAC [ps]		tVAC [ps]		tVAC [ps]	
	min	max	min	max	min	max	min	max
> 2.0	75	-	105	-	93	-	93	-
2.0	57	-	105	-	93	-	93	-
1.5	50	-	80	-	70	-	70	-
1.0	38	-	30	-	25	-	25	-
0.9	34	-	13	-	note	-	note	-
0.8	29	-	note	-	note	-	note	-
0.7	note	-	note	-	note	-		
0.6	note	-	note	-	note	-		
0.5	note	-	note	-	note	-		
< 0.5	note	-	note	-	note	-		

Note: Rising input signal shall become equal to or greater than VIH(AC) level and falling input signal shall become equal to or less than VIL(AC) level.

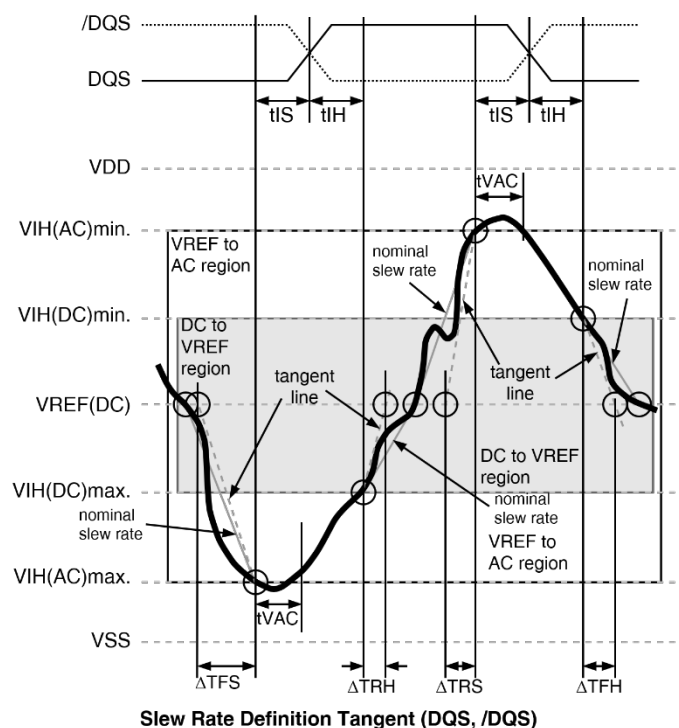
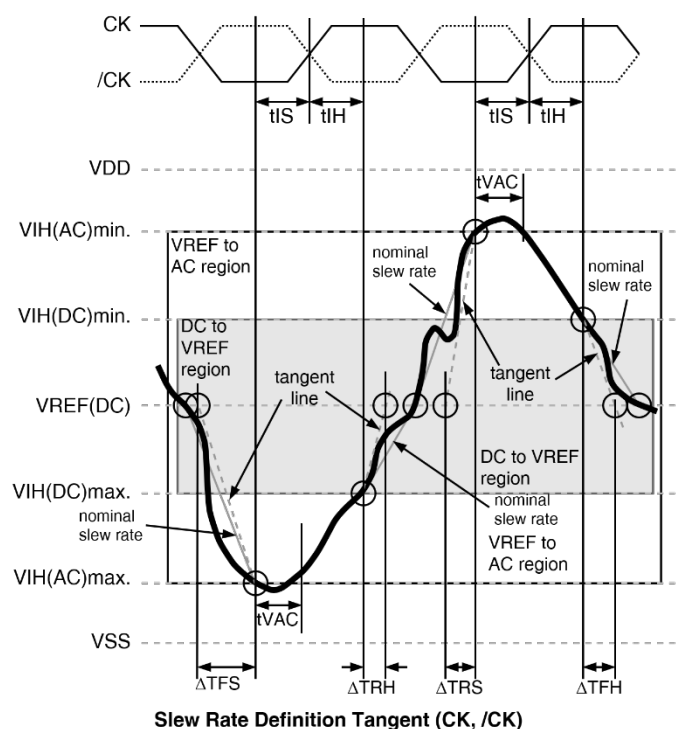


$$\text{Setup slew rate Falling signal} = \frac{VREF(DC) - VIL(AC)max.}{\Delta TFS}$$

$$\text{Hold slew rate Rising signal} = \frac{VREF(DC) - VIL(DC)max.}{\Delta TRH}$$

$$\text{Setup slew rate Rising signal} = \frac{VIH(AC)min. - VREF(DC)}{\Delta TRS}$$

$$\text{Hold slew rate Falling signal} = \frac{VIH(DC)min. - VREF(DC)}{\Delta TFH}$$



$$\text{Setup slew rate Falling signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(AC)_{max.}]}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{\text{tangent line } [V_{IH}(AC)_{min.} - V_{REF}(DC)]}{\Delta TRS}$$

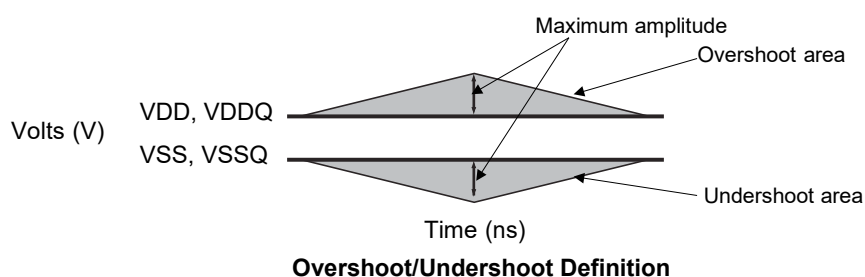
$$\text{Hold slew rate Rising signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(DC)_{max.}]}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{\text{tangent line } [V_{IH}(DC)_{min.} - V_{REF}(DC)]}{\Delta TFH}$$

## 5.7. Overshoot and Undershoot Specifications for DDR3

### 5.7.1. Overshoot and Undershoot Specifications

Pins	Parameter	Specification
Command, Address CKE, ODT	Maximum peak amplitude allowed for overshoot	0.4V
	Maximum peak amplitude allowed for undershoot	0.4V
	Maximum overshoot area above VDD	
	DDR3-1866	0.28V-ns
	DDR3-1600	0.33V-ns
	DDR3-1333	0.4V-ns
	Maximum undershoot area below VSS	
	DDR3-1866	0.28V-ns
	DDR3-1600	0.33V-ns
	DDR3-1333	0.4V-ns
CK, /CK	Maximum peak amplitude allowed for overshoot	0.4V
	Maximum peak amplitude allowed for undershoot	0.4V
	Maximum overshoot area above VDD	
	DDR3-1866	0.11V-ns
	DDR3-1600	0.13V-ns
	DDR3-1333	0.15V-ns
	Maximum undershoot area below VSS	
	DDR3-1866	0.11V-ns
	DDR3-1600	0.13V-ns
	DDR3-1333	0.15V-ns
DQ, DQS, /DQS, DM	Maximum peak amplitude allowed for overshoot	0.4V
	Maximum peak amplitude allowed for undershoot	0.4V
	Maximum overshoot area above VDDQ	
	DDR3-1866	0.11V-ns
	DDR3-1600	0.13V-ns
	DDR3-1333	0.15V-ns
	Maximum undershoot area below VSSQ	
	DDR3-1866	0.11V-ns
	DDR3-1600	0.13V-ns
	DDR3-1333	0.15V-ns



## 5.8. Output Driver DC Electrical Characteristics for DDR3

### 5.8.1. Output Driver Impedance

RON will be achieved by the DDR3 SDRAM after proper I/O calibration. Tolerance and linearity requirements are referred to the Output Driver DC Electrical Characteristics table.

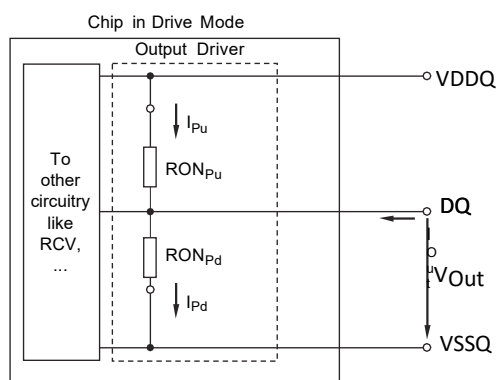
A functional representation of the output buffer is shown in the figure Output Driver: Definition of Voltages and Currents.

RON is defined by the value of the external reference resistor RZQ as follows:

- $RON40 = RZQ/6$
- $RON34 = RZQ/7$

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

Parameter	Symbol	Definition	Conditions
Output driver pull-up impedance	RONPu	$\frac{VDDQ - VOUT}{ IOUT }$	RONPd is turned off
Output driver pull-down impedance	RONPd	$\frac{VOUT}{ IOUT }$	RONPu is turned off



Output Driver: Definition of Voltages and Currents



[RZQ = 240Ω, entire operating temperature range; after proper ZQ calibration]

RZQ = 240Ω, entire operating temperature range, after proper EQ calibration							
RONnom	Resistor	VOUT	min.	nom.	max.	Unit	Note
40Ω	RON40Pd	VOL (DC) = 0.2 × VDDQ	0.6	1.0	1.1	RZQ/6	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.9	1.0	1.4		
	RON40Pu	VOL (DC) = 0.2 × VDDQ	0.9	1.0	1.4	RZQ/6	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.6	1.0	1.1		
34Ω	RON34Pd	VOL (DC) = 0.2 × VDDQ	0.6	1.0	1.1	RZQ/7	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.9	1.0	1.4		
	RON34Pu	VOL (DC) = 0.2 × VDDQ	0.9	1.0	1.4	RZQ/7	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.1		
		VOH (DC) = 0.8 × VDDQ	0.6	1.0	1.1		
Mismatch between pull-up and pull down. MMPuPd		VOM (DC) = 0.5 × VDDQ	-10		10	%	1,2,4

Notes:

- The tolerance limits are specified after calibration with stable voltage and temperature.  
For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
- Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × VDDQ and 0.8 × VDDQ.
- Measurement definition for mismatch between pull-up and pull-down, MMPuPd:

Measure RONPu and RONPd, both at 0.5 × VDDQ:

$$\text{MMPuPd} = \frac{\text{RONPu} - \text{RONPd}}{\text{RONnom}} \times 100$$

### Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the table Output Driver Sensitivity Definition and Output Driver Voltage and Temperature Sensitivity.

$$\Delta T = T - T (@\text{calibration}); \Delta V = VDDQ - VDDQ (@\text{calibration}); VDD = VDDQ$$

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

### [Output Driver Sensitivity Definition]

	min	max	unit
RONPu@VOH(DC)	0.6-dRONdTH x  ΔT  - dRONdVH x  ΔV	1.1+dRONdTH x  ΔT  + dRONdVH x  ΔV	RZQ/7
RON@ VOM (DC)	0.9-dRONdTM x  ΔT  - dRONdVM x  ΔV	1.1+dRONdTM x  ΔT  + dRONdVM x  ΔV	RZQ/7
RONPd@VOL (DC)	0.6-dRONdTL x  ΔT  - dRONdVL x  ΔV	1.1+dRONdTL x  ΔT  + dRONdVL x  ΔV	RZQ/7

### [Output Driver Voltage and Temperature Sensitivity]

	DDR3-1866/1600		DDR3-1333		Unit
	min.	max.	min.	max.	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.13	0	0.15	%/mV
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.13	0	0.15	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.13	0	0.15	%/mV

## 5.9. On-Die Termination (ODT) Levels and I-V Characteristics for DDR3

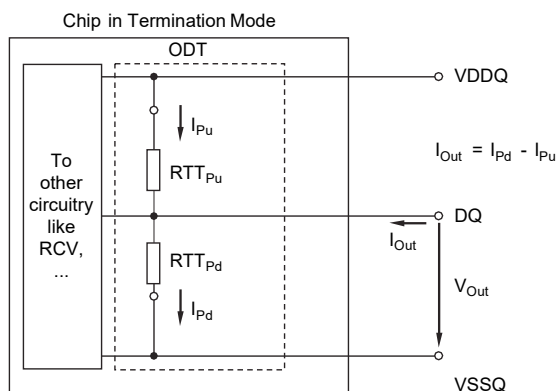
### 5.9.1. On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance  $R_{TT}$  is defined by bits A9, A6 and A2 of the MR1 Register. ODT is applied to the DQ, DM, DQS, /DQS and TDQS, /TDQS (x8 devices only) pins.

A functional representation of the on-die termination is shown in the figure On-Die Termination: Definition of Voltages and Currents.

The individual pull-up and pull-down resistors ( $R_{TTPu}$  and  $R_{TTPd}$ ) are defined as follows:

Parameter	Symbol	Definition	Conditions
ODT pull-up resistance	$R_{TTPu}$	$\frac{VDDQ - V_{OUT}}{ I_{OUT} }$	$R_{TTPd}$ is turned off
ODT pull-down resistance	$R_{TTPd}$	$\frac{V_{OUT}}{ I_{OUT} }$	$R_{TTPu}$ is turned off



### On-Die Termination: Definition of Voltages and Currents

The value of the termination resistor can be set via MRS command to  $R_{TT60} = RZQ/4$  (nom) or  $R_{TT120} = RZQ/2$  (nom).

$R_{TT60}$  or  $R_{TT120}$  will be achieved by the DDR3 SDRAM after proper I/O calibration has been performed. Tolerances requirements are referred to the ODT DC Electrical Characteristics table.

### 5.9.2. Measurement Definition for $R_{TT}$

Apply  $V_{IH}$  (AC) to pin under test and measure current  $I(V_{IH}(AC))$ , then apply  $V_{IL}(AC)$  to pin under test and measure current  $I(V_{IL}(AC))$  respectively.

$$R_{TT} = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

### 5.9.3. Measurement Definition for $\Delta VM$

Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left( \frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

#### 5.9.4. ODT DC Electrical Characteristics

[RZQ = 240Ω, entire operating temperature range; after proper ZQ calibration]

MR1 [A9,A6,A2]	RTT	Resistor	VOUT	min.	nom.	max.	Unit	Notes
[0, 1, 0]	120Ω	RTT120Pd240	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.1		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.4		
		RTT120Pu240	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.4		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.1		
RTT120	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/2	1, 2, 5		
[0, 0, 1]	60Ω	RTT60Pd120	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.1		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/2	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.4		
		RTT60Pu120	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.4		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/2	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.1		
RTT60	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/4	1, 2, 5		
[0, 1.1]	40Ω	RTT40Pd80	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.1		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/3	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.4		
		RTT40Pu80	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.4		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/3	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.1		
RTT40	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/6	1, 2, 5		
[1, 0, 1]	30Ω	RTT30Pd60	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.1		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/4	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.4		
		RTT30Pu60	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.4		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/4	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.1		
RTT30	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/8	1, 2, 5		
[1, 0, 0]	20Ω	RTT20Pd40	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.1		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/6	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.4		
		RTT20Pu40	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.4		
			0.5 x VDDQ	0.9	1.0	1.1	RZQ/6	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.1		
RTT20	VIL (AC) to VIH (AC)	0.9	1.0	1.6	RZQ/12	1, 2, 5		
Deviation of VM w.r.t. VDDQ/2, ΔVM				-5		5	%	1, 2, 5, 6

Notes:

- The tolerance limits are specified after calibration with stable voltage and temperature.  
For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
- Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
- Not a specification requirement, but a design guide line.
- Measurement Definition for RTT:  
Apply VIH (AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.

$$RTT = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

6. Measurement Definition for VM and  $\Delta VM$ :  
Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left( \frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

#### 5.9.5. ODT Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the table ODT Sensitivity Definition and ODT Voltage and Temperature Sensitivity.

$$\Delta T = T - T (@calibration); \Delta V = VDDQ - VDDQ (@calibration); VDD = VDDQ$$

Note: dRTTdT and dRTTdV are not subject to production test but are verified by design and characterization.

##### [ODT Sensitivity Definition]

	min.	max.	unit
RTT	$0.9 - dRTTdT \times  \Delta T  - dRTTdV \times  \Delta V $	$1.6 + dRTTdT \times  \Delta T  + dRTTdV \times  \Delta V $	RZQ/2, 4, 6, 8, 12

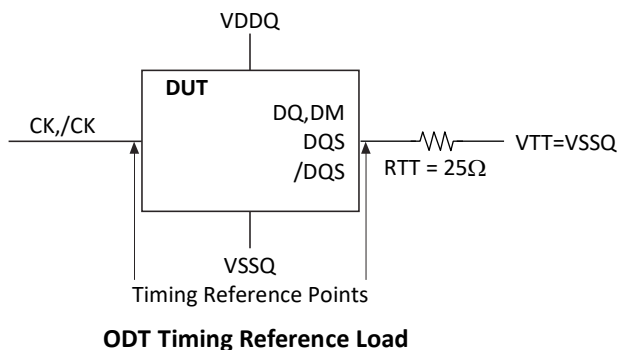
##### [ODT Voltage and Temperature Sensitivity]

	min.	max.	unit
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

## 5.10. ODT Timing Definitions for DDR3

### 5.10.1. Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings are defined in ODT Timing Reference Load.



### 5.10.2. ODT Timing Definitions

Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in the following table and subsequent figures.

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK - /CK defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure a)
tAONPD	Rising edge of CK - /CK with ODT begin first registered high	Extrapolated point at VSSQ	Figure b)
tAOF	Rising edge of CK - /CK defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure c)
tAOFPD	Rising edge of CK - /CK with ODT begin first registered low	End point: Extrapolated point at VRTT_Nom	Figure d)
tADC	Rising edge of CK - /CK defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_WR and VRTT_Nom respectively	Figure e)

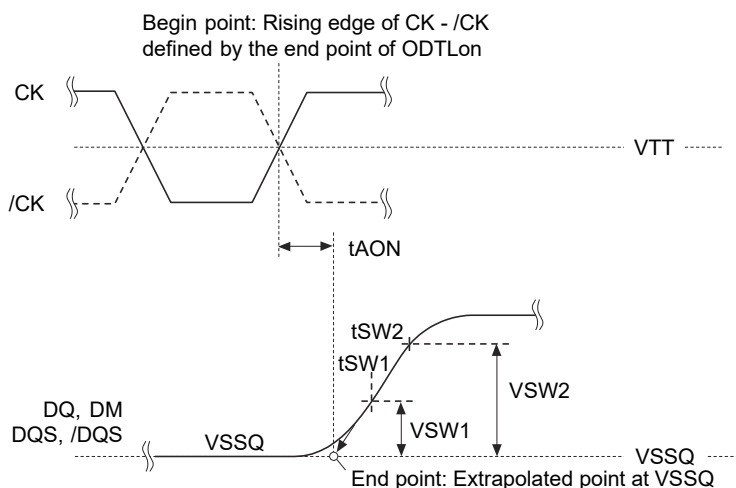
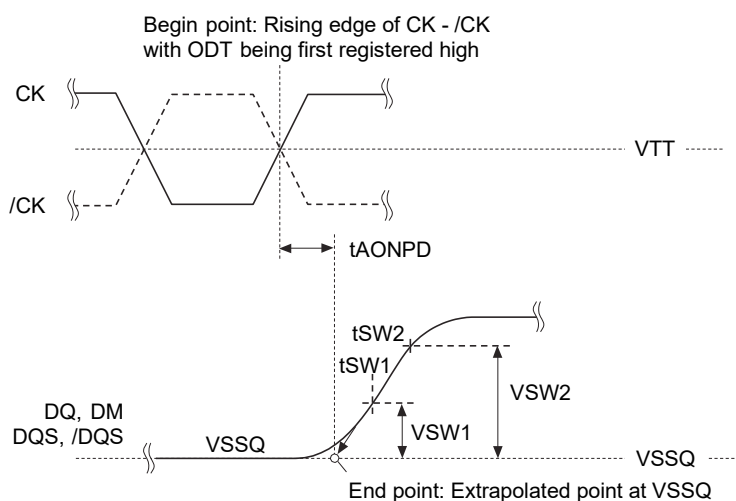
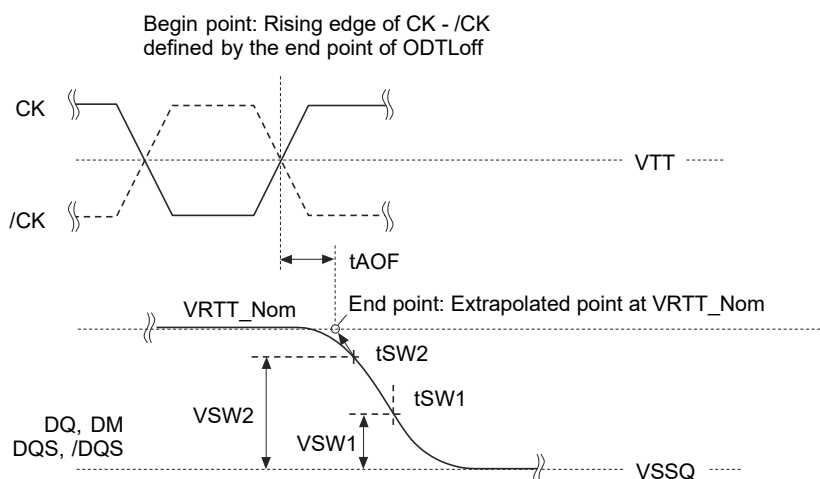


Figure a) Definition of tAON



**Figure b) Definition of tAONPD**



**Figure c) Definition of tAOF**

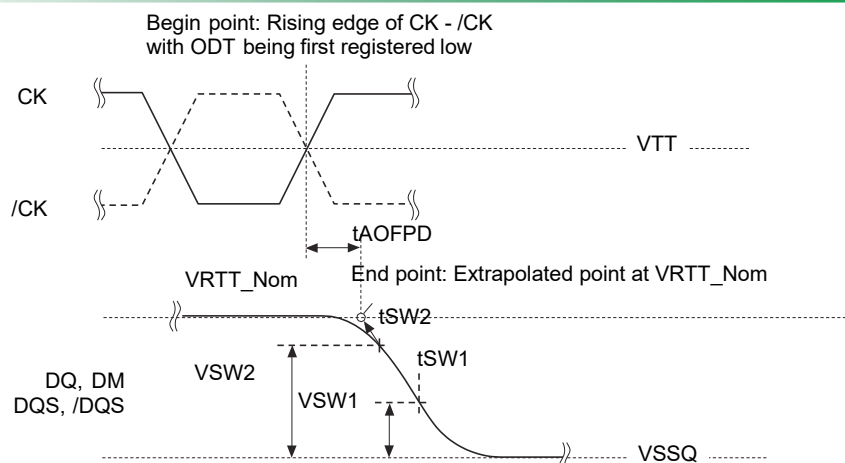


Figure d) Definition of tAOF

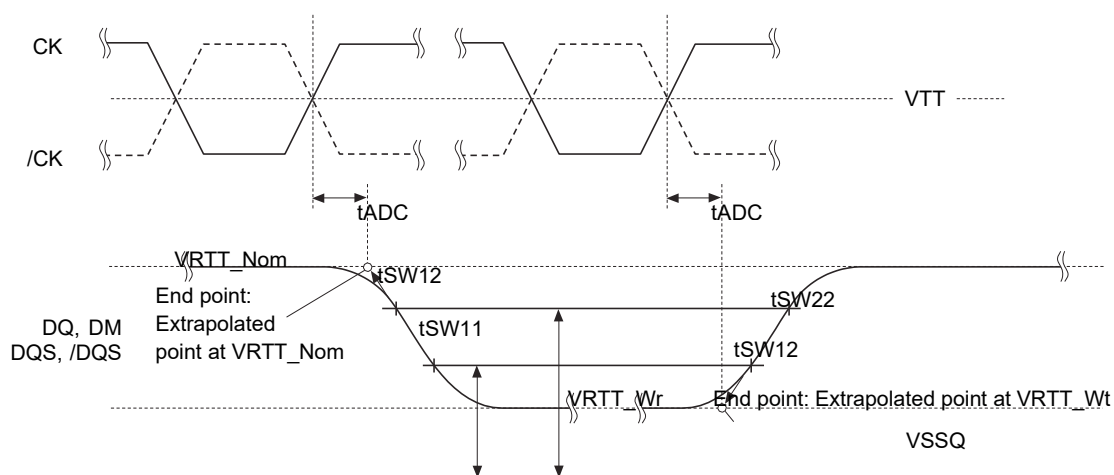


Figure e) Definition of tAOF

### 5.10.3. Reference Settings for ODT Timing Measurements

Measurement reference settings are provided in the following Table.

Measured Parameter	RTT Nom Setting	RTT WR Setting	VSW1 [V]	VSW2 [V]	Note
tAON	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAONPD	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAOF	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAOFPD	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tADC	RZQ/12	RZQ/2	0.20	0.30	



**For DDR3L operation**

**5.11. AC and DC Input Measurement Levels for DDR3L**

**5.11.1. AC and DC Input Levels for Single-Ended Command and Address Signals**

[AC and DC Input Level for Single-Ended Command and Address signals]

Symbol	Parameter	DDR3L-1066		DDR3L-1333/1600		DDR3L-1866		Unit	Notes
		min	max	min	max	min	max		
VIH.CA(DC90)	DC input logic high	VREF + 0.09	VDD	VREF + 0.09	VDD	VREF + 0.09	VDD	V	1
VIL.CA(DC90)	DC input logic low	VSS	VREF - 0.09	VSS	VREF - 0.09	VSS	VREF - 0.09	V	1
VIH.CA(AC160)	AC input logic high	VREF + 0.160	Note 2	VREF + 0.160	Note 2	-	-	V	1, 2, 5
VIL.CA(AC160)	AC input logic low	Note 2	VREF - 0.160	Note 2	VREF - 0.160	-	-	V	1, 2, 5
VIH.CA(AC135)	AC input logic high	VREF + 0.135	Note 2	VREF + 0.135	Note 2	VREF + 0.135	Note 2	V	1, 2, 5
VIL.CA(AC135)	AC input logic low	Note 2	VREF - 0.135	Note 2	VREF - 0.135	Note 2	VREF - 0.135	V	1, 2, 5
VIH.CA(AC125)	AC input logic high	-	-	-	-	VREF + 0.125	Note 2	V	1, 2, 5
VIL.CA(AC125)	AC input logic low	-	-	-	-	Note 2	VREF - 0.125	V	1, 2, 5
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. For input only pins except /RESET, VREF = VREFCA (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFCA (DC) by more than +/-1% VDD (for reference: approx. +/-13.5 mV).
4. For reference: approx. VDD/2 +/-13.5 mV.
5. These levels apply for 1.35V operation only.

**5.11.2. AC and DC Input Levels for Single-Ended Data Signals**

[Single-Ended AC and DC Input Levels for DQ and DM]

Symbol	Parameter	DDR3L-1066		DDR3L-1333/1600		DDR3L-1866		Unit	Notes
		min	max	min	max	min	max		
VIH.DQ(DC90)	DC input logic high	VREF + 0.09	VDD	VREF + 0.09	VDD	VREF + 0.09	VDD	V	1
VIL.DQ(DC90)	DC input logic low	VSS	VREF - 0.09	VSS	VREF - 0.09	VSS	VREF - 0.09	V	1
VIH.DQ(AC160)	AC input logic high	VREF + 0.160	Note 2	-	-	-	-	V	1, 2, 5
VIL.DQ(AC160)	AC input logic low	Note 2	VREF - 0.160	-	-	-	-	V	1, 2, 5
VIH.DQ(AC135)	AC input logic high	VREF + 0.135	Note 2	VREF + 0.135	Note 2	-	-	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note 2	VREF - 0.135	Note 2	VREF - 0.135	-	-	V	1, 2, 5
VIH.CA(AC130)	AC input logic high	-	-	-	-	VREF + 0.130	Note 2	V	1, 2, 5
VIL.CA(AC130)	AC input logic low	-	-	-	-	Note 2	VREF - 0.130	V	1, 2, 5
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

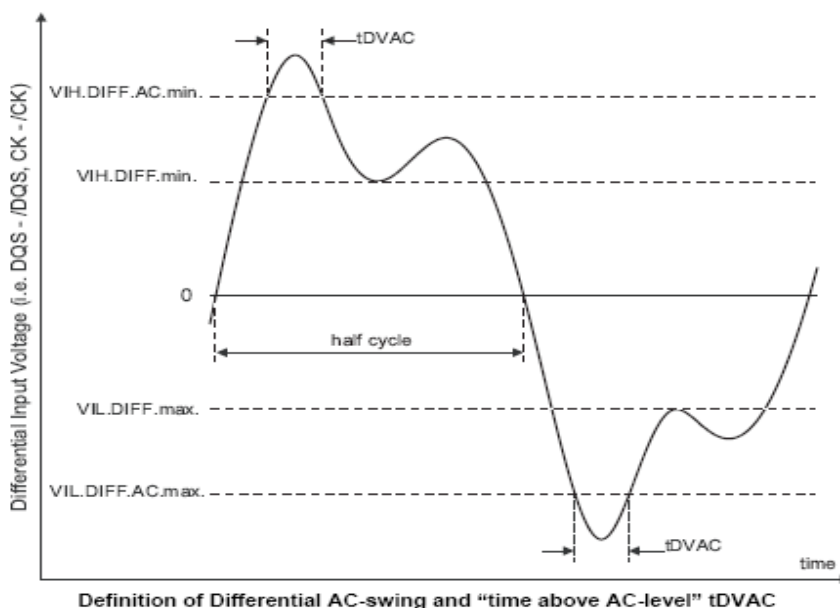
1. For input only pins except /RESET, VREF = VREFDQ (DC).
2. See Overshoot and Undershoot Specifications section.
3. The AC peak noise on VREF may not allow VREF to deviate from VREFDQ (DC) by more than +/-1% VDD (for reference: approx. +/-13.5 mV).
4. For reference: approx. VDD/2 +/-13.5 mV.
5. These levels apply for 1.35V operation only.

**5.11.3. VREF Tolerances**

See 5.4.3 VREF Tolerances section

#### 5.11.4. AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Differential swing requirements for clock (CK - /CK) and strobe (DQS - /DQS)  
[Differential AC and DC Input Levels]

Symbol	Parameter	DDR3L-1333/1600/1866		Unit	Notes
		min	max		
VIHdiff	Differential input high	+ 0.180	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.180	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
VILdiff(ac)	Differential input low ac	Note 3	2 x (VIL(ac) - Vref)	V	2

NOTE:

- Used to define a differential signal slew-rate.
- For CK - /CK use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - /DQS, DQSL, /DQSL, DQSU, /DQSU use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined; however, the single-ended signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

### [Allowed time before ringback (tDVAC) for CK - /CK and DQS - /DQS]

Slew Rate [V/ns]	DDR3L-1333/1600				DDR3L-1866					
	tDVAC [ps] @ [VIH/Ldiff(AC)] = 320mV		tDVAC [ps] @ [VIH/Ldiff(AC)] = 270mV		tDVAC [ps] @ [VIH/Ldiff(AC)] = 270mV		tDVAC [ps] @ [VIH/Ldiff(AC)] = 250mV		tDVAC [ps] @ [VIH/Ldiff(AC)] = 260mV	
	min	max	min	max	min	max	min	max	min	max
> 4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134	-	95	-	105	-	111	-
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	note	-	44	-	5	-	22	-	24	-
1.0	note	-	note	-	note	-	note	-	note	-
< 1.0	note	-	note	-	note	-	note	-	note	-

Note: Rising input differential signal shall become equal to or greater than VIHdiff(AC) level and falling input differential signal shall become equal to or less than VILdiff(AC) level.

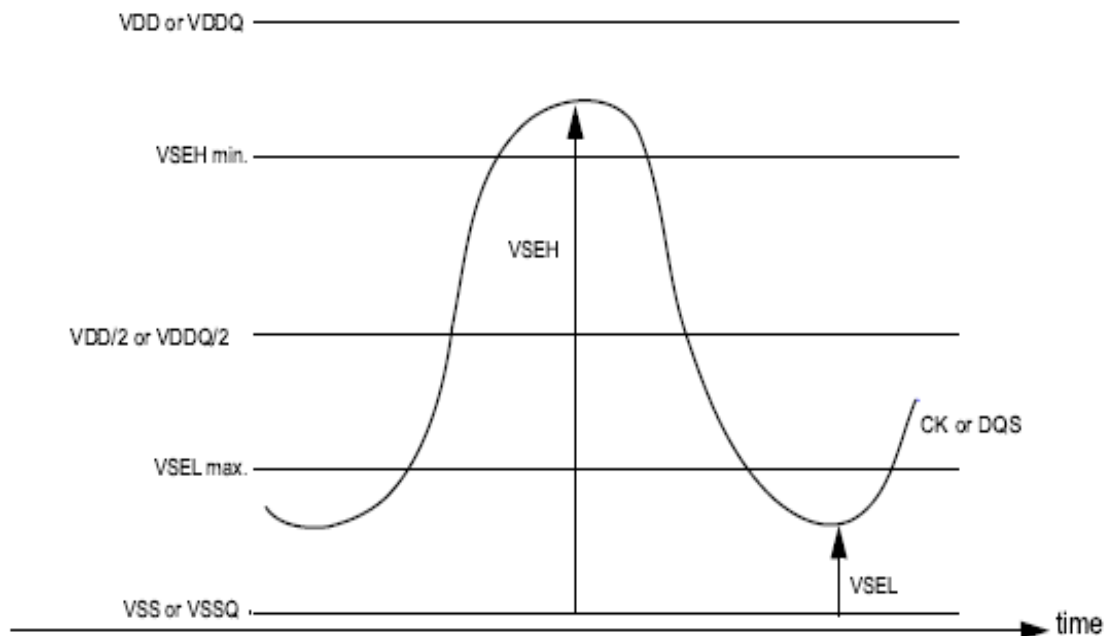
### Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU) has also to comply with certain requirements for single-ended signals.

CK and /CK have to reach VSEH min. / VSEL max. (approximately equal to the AC-levels (VIH(AC) / VIL(AC)) for Address/command signals) in every half-cycle.

DQS, DQSL, DQSU, /DQS, /DQSL, /DQSU have to reach VSEH min./VSEL max. (approximately equal to the AC-levels (VIH(AC) / VIL(AC)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for Address/command and DQ's might be different per speed-bin etc. E.g. if VIH 150 (AC)/VIL 150 (AC) is used for Address/command signals, then these ac-levels apply also for the single ended components of differential CK and /CK.



### Single-Ended Requirement for Differential Signals.

Note that while Address/command and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL max, VSEH min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

#### [Single-ended levels for CK, DQS, DQSL, DQSU, /CK, /DQS, /DQSL or /DQSU]

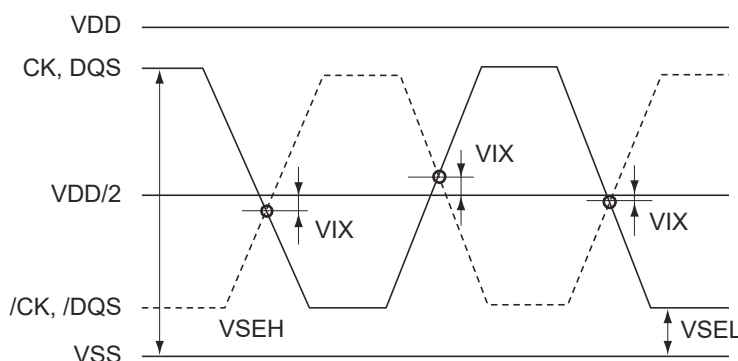
Symbol	Parameter	DDR3L-1333/1600/1866		Unit	Notes
		min	max		
VSEH	Single-ended high level for strobes	$(VDD / 2) + 0.175$	Note 3	V	1,2
	Single-ended high level for CK, /CK	$(VDD / 2) + 0.175$	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	$(VDD / 2) - 0.175$	V	1,2
	Single-ended low level for CK, /CK	Note 3	$(VDD / 2) - 0.175$	V	1,2

Notes:

- For CK, /CK use VIH/VIL(AC) of ADD/CMD; for strobes (DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU) use VIH/VIL(AC) of DQs.
- VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single ended components of differential signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Overshoot and Undershoot specifications.

#### 5.11.5. Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, /CK and DQS, /DQS) must meet the requirements in table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



VIX Definition

#### [Cross point voltage for differential input signals (CK, DQS)]

Symbol	Parameter	DDR3L-1333/1600/1866		Unit	Notes
		min	max		
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV	1
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV	

Notes:

- The relation between VIX min./max. and VSEL/VSEH should satisfy following.  
 $(VDD/2) + VIX (\text{min.}) - VSEL \geq 25\text{mV}$   
 $VSEH - ((VDD/2) + VIX (\text{max.})) \geq 25\text{mV}$

#### 5.11.6. Slew Rate Definitions for Differential Input Signals

See 5.4.5 Slew Rate Definitions for Differential Input Signals section

## 5.12. AC and DC Output Measurement Levels for DDR3L

### 5.12.1. Single Ended AC and DC Output Levels

See 5.5.1 Single Ended AC and DC Output Levels section

### 5.12.2. Differential AC and DC Output Levels

See 5.5.2 Differential AC and DC Output Levels section

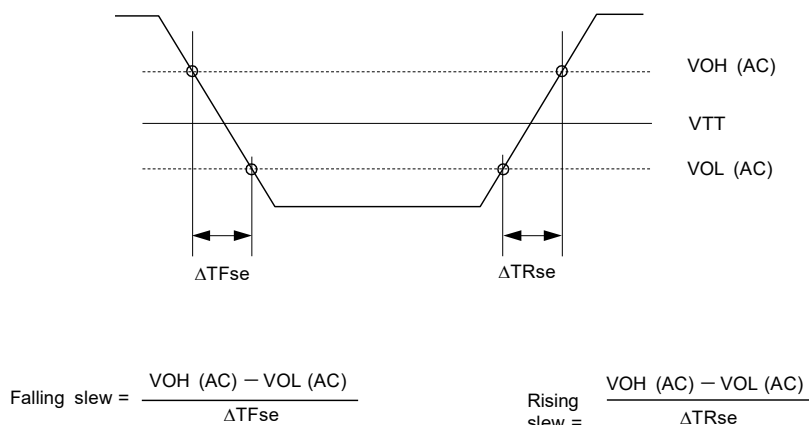
### 5.12.3. Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as below.

#### [Single-ended Output Slew Rate Definition]

Description	Measured		Defined by
	from	to	
Output slew rate for rising edge	VOL (AC)	VOH (AC)	$\frac{VOH(AC) - VOL(AC)}{\Delta TRse}$
Output slew rate for falling edge	VOH (AC)	VOL (AC)	$\frac{VOH(AC) - VOL(AC)}{\Delta TFse}$

NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.



#### Output Slew Rate Definition for Single-Ended Signals

#### [Output Slew Rate (Single-ended)]

Parameter	Symbol	Speed	min.	max.	Unit
Single-ended Output Slew Rate	SRQse	DDR3-1866	1.75	5	V/ns
		DDR3-1600	1.75	5	
		DDR3-1333	1.75	5	

Remark: SR = slew rate. se = single-ended signals. Q = Query output

Note: 1. In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

- (a) is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
- (b) is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5V/ns applies.

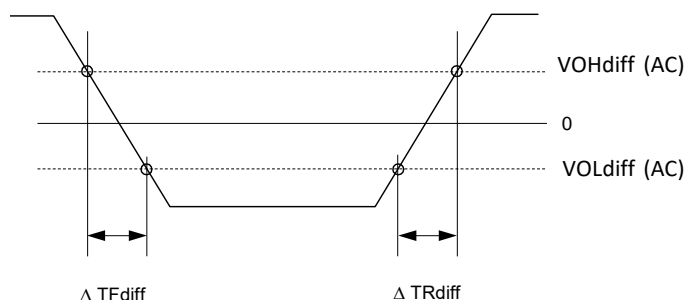
#### 5.12.4. Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as below.

##### [Differential Output Slew Rate Definition]

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff (AC)	VOHdiff (AC)	$\frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TRdiff}$
Differential output slew rate for falling edge	VOHdiff (AC)	VOLdiff (AC)	$\frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TFdiff}$

NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.



$$\text{Falling slew} = \frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TFdiff}$$

$$\text{Rising slew} = \frac{VOHdiff(AC) - VOLdiff(AC)}{\Delta TRdiff}$$

#### Differential Output Slew Rate Definition

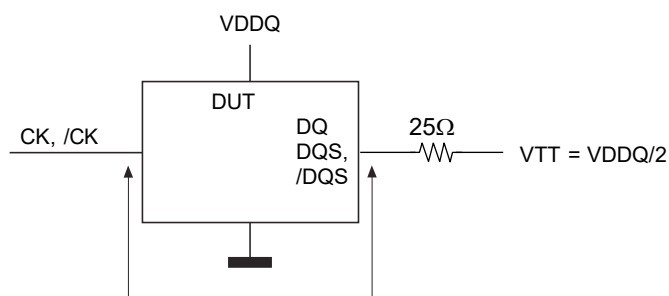
##### [Differential Output Slew Rate]

Parameter	Symbol	Speed	min.	max.	Unit
Differential Output Slew Rate	SRQdiff	DDR3-1866	3.5	12	V/ns
		DDR3-1600	3.5	12	
		DDR3-1333	3.5	12	

Remark: SR = slew rate. diff = differential signals. Q = Query output. For Ron = RZQ/7 setting

#### 5.12.5. Reference Load for AC Timing and Output Slew Rate

This figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.



Reference Output Load

#### 5.12.6. Reference Load for AC Timing and Output Slew Rate

See 5.5.5 Reference Load for AC Timing and Output Slew Rate section

### 5.12.7. DQS Output Cross point voltage

#### [DDR3L-1333 VOX]

Symbol	Parameter		DQS, /DQS Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
Vox	Deviation of DQS,/DQS output cross point voltage from 0.5 * VDDQ	max	+115	+130	+195	+205	+205	+205	+205	+205	+205	mV
		min	-115	-130	-160	-195	-205	-205	-205	-205	-205	mV

Note:

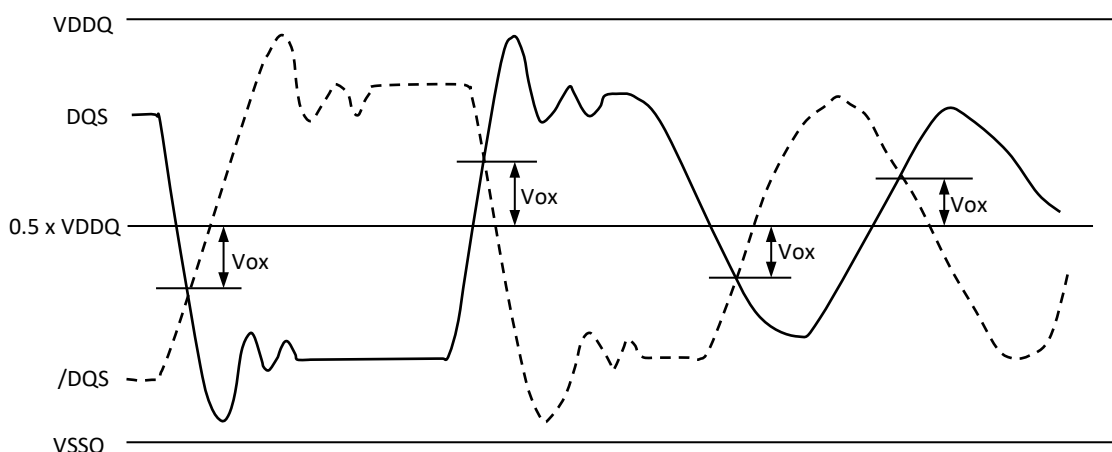
1. Measured using an effective test load of 25  $\Omega$  to 0.5\*VDDQ at each of the differential outputs.
2. For a differential slew rate in between the listed values, the VOX value may be obtained by linear interpolation.
3. Refer to Figure Y for reference drawing, DQS/DQS# shown single-ended for measurement point.
4. The DQS/DQS# pins under test are not required to be able to drive each of the slew rates listed in the table; the pins under test will provide one VOX value when tested with specified test condition. The DQS and DQS# differential slew rate when measuring VOX determines which VOX limits to use.

#### [DDR3L-1600/1866 VOX]

Symbol	Parameter		DQS, /DQS Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
Vox	Deviation of DQS,/DQS output cross point voltage from 0.5 * VDDQ	max	+90	+105	+133	+155	+180	+205	+205	+205	+205	mV
		min	-90	-105	-133	-155	-180	-205	-205	-205	-205	mV

Note:

1. Measured using an effective test load of 25  $\Omega$  to 0.5\*VDDQ at each of the differential outputs.
2. For a differential slew rate in between the listed values, the VOX value may be obtained by linear interpolation.
3. Refer to Figure Y for reference drawing, DQS/DQS# shown single-ended for measurement point.
4. The DQS/DQS# pins under test are not required to be able to drive each of the slew rates listed in the table; the pins under test will provide one VOX value when tested with specified test condition. The DQS and DQS# differential slew rate when measuring VOX determines which VOX limits to use.



Definition of Output cross point voltage for DQS and /DQS

### 5.13. Address / Command /Data Setup, Hold and Derating for DDR3L

For all input signals the total tIS, tDS (setup time) and tIH, tDH (hold time) required is calculated by adding the data sheet tIS (base), tDS (base) and tIH (base), tDH (base) value to the  $\Delta tIS$ ,  $\Delta tDS$  and  $\Delta tIH$ ,  $\Delta tDH$  derating value respectively.

Example: tDS (total setup time) = tDS (base) +  $\Delta tDS$ .

Setup (tIS, tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF (DC) and the first crossing of VIH (AC) min. Setup (tIS, tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF (DC) and the first crossing of VIL (AC) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF (DC) to AC region', use nominal slew rate for derating value (See the figure of Slew Rate Definition Nominal).

If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF (DC) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see the figure of Slew Rate Definition Tangent).

Hold (tIH, tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (DC) max. and the first crossing of VREF (DC). Hold (tIH, tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH (DC) min. and the first crossing of VREF (DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to VREF (DC) region', use nominal slew rate for derating value (See the figure of Slew Rate Definition Nominal).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF (DC) region', the slew rate of a tangent line to the actual signal from the DC level to VREF (DC) level is used for derating value (see the figure of Slew Rate Definition Tangent).

For a valid transition the input signal has to remain above/below VIH/VIL(AC) for some time tVAC (see the table of Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL (AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL (AC).

For slew rates in between the values listed in the tables below, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

#### [Address/Command Setup and Hold Base-Values for 1V/ns]

	DDR3-1866	DDR3-1600	DDR3-1333	Unit	note	Reference
tIS(base) AC160	-	60	80	ps	1	VIH/VIL(AC)
tIS(base) AC135	65	185	205	ps	1,2	VIH/VIL(AC)
tIS(base) AC125	150	-	-	ps	1,3	VIH/VIL(AC)
tIH(base) DC90	110	130	150	ps	1	VIH/VIL(AC)

#### Notes:

1. AC/DC referenced for 1V/ns Address/Command slew rate and 2V/ns differential CK, /CK slew rate.
2. The tIS (base) AC135 specifications are adjusted from the tIS(base) AC160 specification by adding an additional 125ps for DDR3L-1066 or 100ps for DDR3L-1600/1333 of derating to accommodate for the lower alternate threshold of 135mV and another 25ps to account for the earlier reference point [(160mV -135mV) / 1V/ns]
3. The tIS (base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps for DDR3L-1866 of derating to accommodate for the lower alternate threshold of 135mV and another 10 ps to account for the earlier reference point [(135mV -125mV) / 1V/ns]



### [Derating values DDR3L-1066/1333/1600 tIS/tIH – AC/DC based]

<div><math>\Delta t_{IS}, \Delta t_{IH}</math> derating in [ps] AC/DC based</div> <div>AC160 Threshold -&gt; <math>V_{IH}(AC) = V_{REF}(DC) + 160\text{ mV}</math>, <math>V_{IL}(AC) = V_{REF}(DC) - 160\text{ mV}</math></div>																	
		CK, /CK Single-ended AC and DC Ou															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$	$\Delta t_{IS}$	$\Delta t_{IH}$
CMD/ ADD Slew rate V/ns	2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5	

### [Derating values DDR3L-1066/1333/1600 tIS/tIH – AC/DC based Alternate AC135 Threshold]

△tIS, △tIH derating in [ps] AC/DC based Alternate AC135 Threshold -> VIH(AC) = VREF(DC) + 135 mV, VIL(AC) = VREF(DC) - 135 mV																	
		CK, /CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD/ ADD Slew rate V/ns	2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5	

**[Derating values DDR3L-1866 tIS/tIH – AC/DC based Alternate AC125 Threshold]**

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based Alternate AC125 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 125\text{ mV}$ , $V_{IL}(AC) = V_{REF}(DC) - 125\text{ mV}$																	
		CK, /CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$	$\Delta tIS$	$\Delta tIH$
CMD/ ADD Slew rate V/ns	2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
	1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	4	40	-4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

**Required time tVAC above VIH(AC) {below VIL(AC)} for valid ADD/CMD transition**

Slew Rate [V/ns]	DDR3L-1333/1600				DDR3L-1866			
	tVAC @ 160 mV [ps]		tVAC @ 135 mV [ps]		tVAC @ 135 mV [ps]		tVAC @ 125 mV [ps]	
	min	max	min	max	min	max	min	max
> 2.0	200	-	213	-	200	-	205	-
2.0	200	-	213	-	200	-	205	-
1.5	173	-	190	-	178	-	184	-
1.0	120	-	145	-	133	-	143	-
0.9	102	-	130	-	118	-	129	-
0.8	80	-	111	-	99	-	111	-
0.7	51	-	87	-	75	-	89	-
0.6	13	-	55	-	43	-	59	-
0.5	note	-	10	-	note	-	18	-
< 0.5	note	-	10	-	note	-	18	-

Note: Rising input signal shall become equal to or greater than VIH(AC) level and falling input signal shall become equal to or less than VIL(AC) level.

[Data Setup and Hold Base-Values]

Symbol	Reference	DDR3L-1866	DDR3L-1600	DDR3L-1333	DDR3L-1066	Units	Notes
tDS(base) AC160	VIH/L(AC) : SR = 1V/ns	-	-	-	40	ps	1
tDS(base) AC135	VIH/L(AC) : SR = 1V/ns	-	25	45	90	ps	1
tDS(base) AC130	VIH/L(AC) : SR = 2V/ns	70	-	-	-	ps	2
tDH(base) DC90	VIH/L(DC) : SR = 2V/ns	75	-	-	-	ps	2
tDH(base) DC90	VIH/L(DC) : SR = 1V/ns	-	55	75	110	ps	1

Notes:

1. AC/DC referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate
2. AC/DC referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate

[Derating values for DDR3L-1066 tDS/tDH – AC/DC based]

$\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based AC160 Threshold $\rightarrow VIH(AC) = VREF(DC) + 160\text{ mV}$ , $VIL(AC) = VREF(DC) - 160\text{ mV}$																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$
DQ Slew rate V/ns	2.0	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

[Derating values for DDR3L-1066/1333/1600 tDS/tDH (AC135)]

$\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based Alternate AC135 Threshold $\rightarrow VIH(AC) = VREF(DC) + 135\text{ mV}$ , $VIL(AC) = VREF(DC) - 135\text{ mV}$																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$
DQ Slew rate V/ns	2.0	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

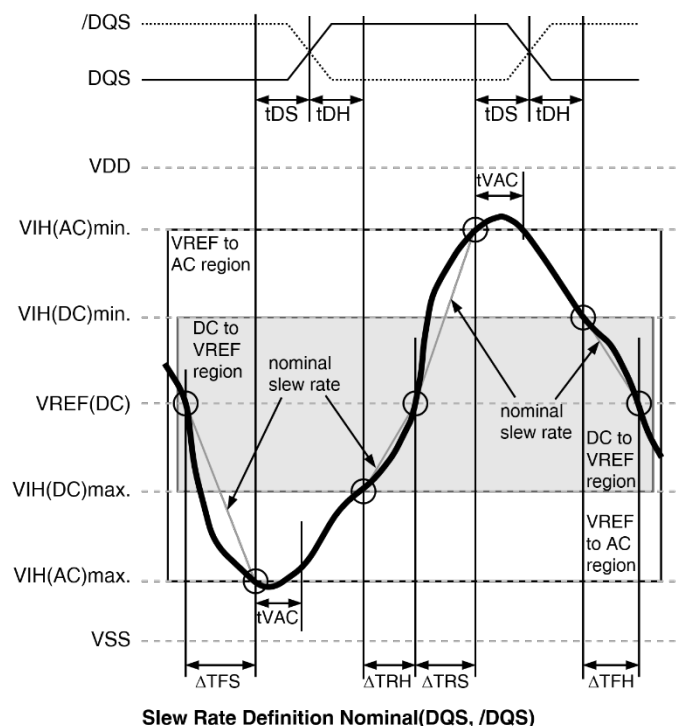
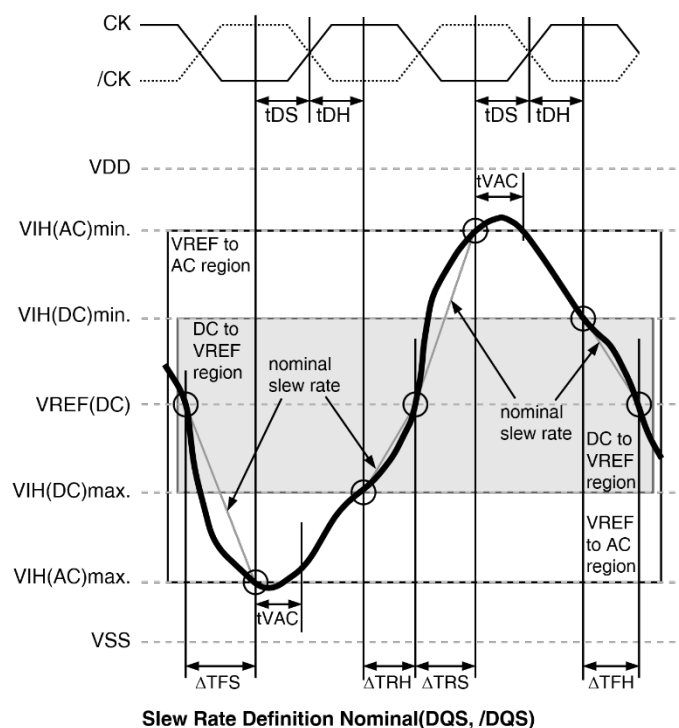
[Derating values for DDR3L-1866 tDS/tDH (AC130)]

$\Delta tDS, \Delta tDH$ derating in [ps] AC/DC based Alternate AC130 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 130 \text{ mV}$ , $V_{IL}(AC) = V_{REF}(DC) - 130 \text{ mV}$																											
		DQS, /DQS Differential Slew Rate																									
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns			
		$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$	$\Delta tDS$	$\Delta tDH$
DQ Slew rate V/ns	4.0	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8	-	-
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15	-	-
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25	-	-
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40	-	-

[Required time tVAC above VIH(AC) {below VIL(AC)} fro valid DQ transition]

Slew Rate [V/ns]	DDR3L-1066 (AC160)		DDR3L-1066/1333/1600 (AC135)		DDR3L-1866 (AC130)	
	tVAC [ps]		tVAC [ps]		tVAC [ps]	
	min	max	min	max	min	max
> 2.0	165	-	113	-	95	-
2.0	165	-	113	-	95	-
1.5	138	-	90	-	73	-
1.0	85	-	45	-	30	-
0.9	67	-	30	-	16	-
0.8	45	-	11	-	note	-
0.7	16	-	note	-	-	-
0.6	note	-	note	-	-	-
0.5	note	-	note	-	-	-
< 0.5	note	-	note	-	-	-

Note: Rising input signal shall become equal to or greater than VIH(AC) level and falling input signal shall become equal to or less than VIL(AC) level.

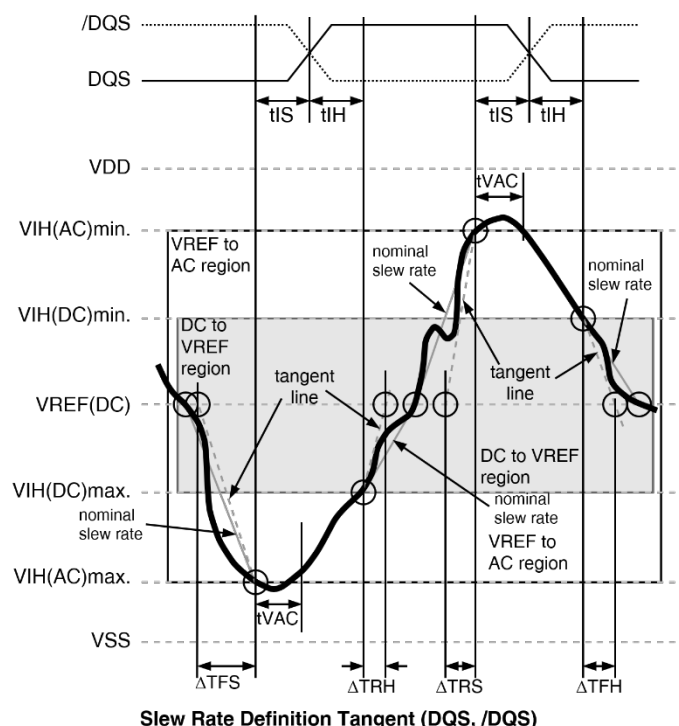
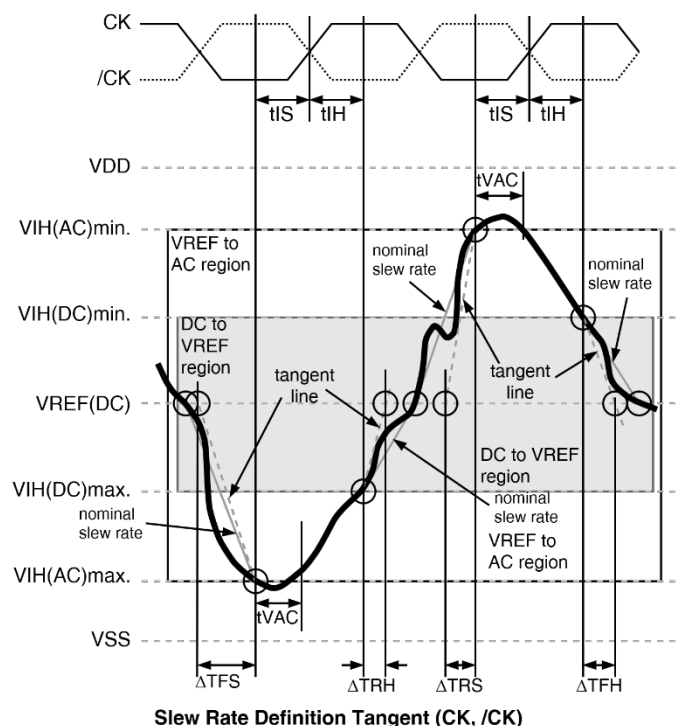


$$\text{Setup slew rate Falling signal} = \frac{VREF(DC) - VIL(AC)max.}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{VIH(AC)min. - VREF(DC)}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{VREF(DC) - VIL(DC)max.}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{VIH(DC)min. - VREF(DC)}{\Delta TFH}$$



$$\text{Setup slew rate Falling signal} = \frac{\text{tangent line [VREF (DC) - VIL (AC) max.]}}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{\text{tangent line [VIH (AC) min. - VREF (DC)]}}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{\text{tangent line [VREF (DC) - VIL (DC) max.]}}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{\text{tangent line [VIH (DC) min. - VREF (DC)]}}{\Delta TFH}$$

## 5.14. Overshoot and Undershoot Specifications for DDR3L

### 5.14.1. Overshoot and Undershoot Specifications

See 5.7.1 Overshoot and Undershoot Specifications section

## 5.15. Output Driver DC Electrical Characteristics for DDR3

### 5.15.1. Output Driver Impedance

RON will be achieved by the DDR3 SDRAM after proper I/O calibration. Tolerance and linearity requirements are referred to the Output Driver DC Electrical Characteristics table.

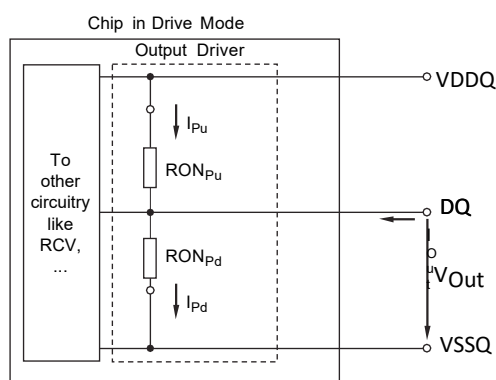
A functional representation of the output buffer is shown in the figure Output Driver: Definition of Voltages and Currents.

RON is defined by the value of the external reference resistor RZQ as follows:

- $RON40 = RZQ/6$
- $RON34 = RZQ/7$

The individual pull-up and pull-down resistors ( $RON_{Pu}$  and  $RON_{Pd}$ ) are defined as follows:

Parameter	Symbol	Definition	Conditions
Output driver pull-up impedance	$RON_{Pu}$	$\frac{VDDQ - VOUT}{ IOUT }$	$RON_{Pd}$ is turned off
Output driver pull-down impedance	$RON_{Pd}$	$\frac{VOUT}{ IOUT }$	$RON_{Pu}$ is turned off



Output Driver: Definition of Voltages and Currents

[RZQ = 240Ω, entire operating temperature range; after proper ZQ calibration]

RZQ = 240Ω, entire operating temperature range, after proper ZQ calibration							
RONom	Resistor	VOUT	min.	nom.	max.	Unit	Note
40Ω	RON40Pd	VOL (DC) = 0.2 × VDDQ	0.6	1.0	1.15	RZQ/6	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.15		
		VOH (DC) = 0.8 × VDDQ	0.9	1.0	1.45		
	RON40Pu	VOL (DC) = 0.2 × VDDQ	0.9	1.0	1.45	RZQ/6	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.15		
		VOH (DC) = 0.8 × VDDQ	0.6	1.0	1.15		
34Ω	RON34Pd	VOL (DC) = 0.2 × VDDQ	0.6	1.0	1.15	RZQ/7	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.15		
		VOH (DC) = 0.8 × VDDQ	0.9	1.0	1.45		
	RON34Pu	VOL (DC) = 0.2 × VDDQ	0.9	1.0	1.45	RZQ/7	1,2,3
		VOM (DC) = 0.5 × VDDQ	0.9	1.0	1.15		
		VOH (DC) = 0.8 × VDDQ	0.6	1.0	1.15		
Mismatch between pull-up and pull down, MMPuPd		VOM (DC) = 0.5 × VDDQ	-10		10	10	1,2,4

Notes:

- The tolerance limits are specified after calibration with stable voltage and temperature.  
For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
- Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × VDDQ and 0.8 × VDDQ.
- Measurement definition for mismatch between pull-up and pull-down, MMPuPd:  
Measure RONPu and RONPd, both at 0.5 × VDDQ:

$$MMPuPd = \frac{RONPu - RONPd}{RONom} \times 100$$

### Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the table Output Driver Sensitivity Definition and Output Driver Voltage and Temperature Sensitivity.

$$\Delta T = T - T (@calibration); \Delta V = VDDQ - VDDQ (@calibration); VDD = VDDQ$$

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

### [Output Driver Sensitivity Definition]

	min	max	unit
RONPu@VOH(DC)	0.6-dRONdTH ×  ΔT  - dRONdVH ×  ΔV	1.1+dRONdTH ×  ΔT  + dRONdVH ×  ΔV	RZQ/7
RON@VOM (DC)	0.9-dRONdTM ×  ΔT  - dRONdVM ×  ΔV	1.1+dRONdTM ×  ΔT  + dRONdVM ×  ΔV	RZQ/7
RONPd@VOL (DC)	0.6-dRONdTL ×  ΔT  - dRONdVL ×  ΔV	1.1+dRONdTL ×  ΔT  + dRONdVL ×  ΔV	RZQ/7

### [Output Driver Voltage and Temperature Sensitivity]

	DDR3-1866/1600		DDR3-1333		Unit
	min.	max.	min.	max.	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.13	0	0.15	%/mV
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.13	0	0.15	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.13	0	0.15	%/mV

## 5.16. On-Die Termination (ODT) Levels and I-V Characteristics for DDR3

### 5.16.1. On-Die Termination (ODT) Levels and I-V Characteristics

See 5.9.1 Output Driver Impedance section



**5.16.2. Measurement Definition for RTT**

See 5.9.2 Measurement Definition for RTT section

**5.16.3. Measurement Definition for  $\Delta VM$**

See 5.9.3 Measurement Definition for  $\Delta VM$  section

#### 5.16.4. ODT DC Electrical Characteristics

[RZQ = 240Ω, entire operating temperature range; after proper ZQ calibration]

MR1 [A9,A6,A2]	RTT	Resistor	VOUT	min.	nom.	max.	Unit	Notes
[0, 1, 0]	120Ω	RTT120Pd240	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.15		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.45		
		RTT120Pu240	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.45		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.15		
RTT120	VIL (AC) to VIH (AC)	0.9	1.0	1.65	RZQ/2	1, 2, 5		
[0, 0, 1]	60Ω	RTT60Pd120	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.15		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/2	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.45		
		RTT60Pu120	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.45		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/2	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.15		
RTT60	VIL (AC) to VIH (AC)	0.9	1.0	1.65	RZQ/4	1, 2, 5		
[0, 1.1]	40Ω	RTT40Pd80	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.15		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/3	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.45		
		RTT40Pu80	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.45		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/3	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.15		
RTT40	VIL (AC) to VIH (AC)	0.9	1.0	1.65	RZQ/6	1, 2, 5		
[1, 0, 1]	30Ω	RTT30Pd60	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.15		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/4	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.45		
		RTT30Pu60	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.45		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/4	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.15		
RTT30	VIL (AC) to VIH (AC)	0.9	1.0	1.65	RZQ/8	1, 2, 5		
[1, 0, 0]	20Ω	RTT20Pd40	VOL (DC) , 0.2 x VDDQ	0.6	1.0	1.15		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/6	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.9	1.0	1.45		
		RTT20Pu40	VOL (DC) , 0.2 x VDDQ	0.9	1.0	1.45		
			0.5 x VDDQ	0.9	1.0	1.15	RZQ/6	1, 2, 3, 4
			VOH (DC) , 0.8 x VDDQ	0.6	1.0	1.15		
RTT20	VIL (AC) to VIH (AC)	0.9	1.0	1.65	RZQ/12	1, 2, 5		
Deviation of VM w.r.t. VDDQ/2, ΔVM				-5		5	%	1, 2, 5, 6

Notes:

- The tolerance limits are specified after calibration with stable voltage and temperature.  
For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
- The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
- Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
- Not a specification requirement, but a design guide line.
- Measurement Definition for RTT:  
Apply VIH (AC) to pin under test and measure current I(VIH(AC)), then apply VIL(AC) to pin under test and measure current I(VIL(AC)) respectively.  

$$RTT = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$
- Measurement Definition for VM and ΔVM:

Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left( \frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

#### 5.16.5. ODT Temperature and Voltage Sensitivity

See 5.9.5 ODT Temperature and Voltage Sensitivity section

### 5.17. ODT Timing Definitions for DDR3

#### 5.17.1. Test Load for ODT Timings

See 5.10.1 ODT Temperature and Voltage Sensitivity section

#### 5.17.2. ODT Timing Definitions

See 5.10.2 ODT Temperature and Voltage Sensitivity section

#### 5.17.3. Reference Settings for ODT Timing Measurements

Measurement reference settings are provided in the following Table.

Measured Parameter	RTT Nom Setting	RTT WR Setting	VSW1 [V]	VSW2 [V]	Note
tAON	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAONPD	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAOF	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tAOFPD	RZQ/4	N/A	0.05	0.10	
	RZQ/12	N/A	0.10	0.20	
tADC	RZQ/12	RZQ/2	0.20	0.25	

## 5.18. IDD and IDDQ Specification Parameters and Test Conditions

### 5.18.1. IDD Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

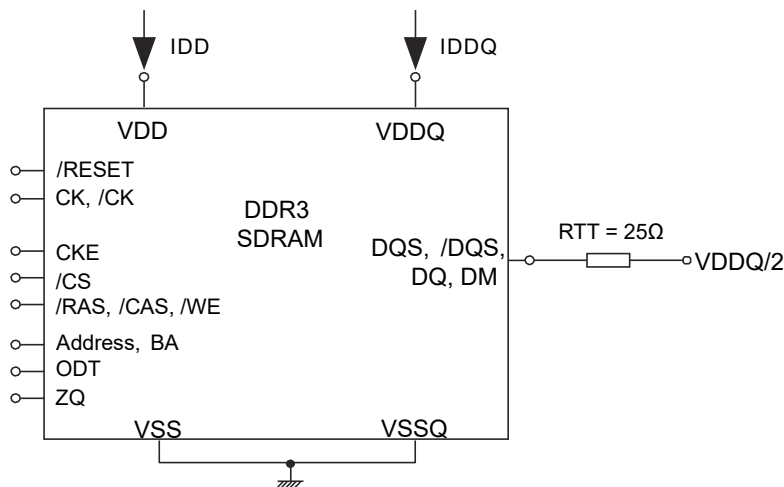
The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.  
Note: IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in figure Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement.

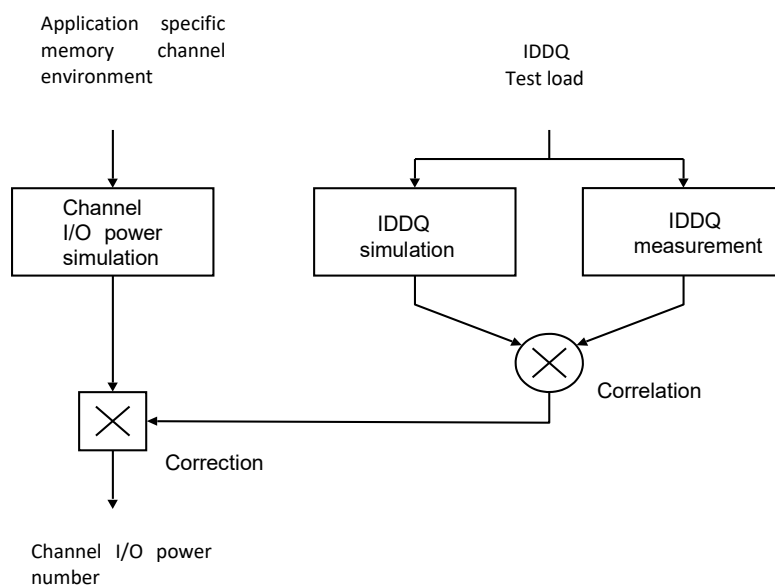
For IDD and IDDQ measurements, the following definitions apply:

- L and 0:  $V_{IN} \leq V_{IL} (AC)(\max)$
- H and 1:  $V_{IN} \geq V_{IH} (AC)(\min)$
- MID-LEVEL: defined as inputs are  $V_{REF} = V_{DDQ} / 2$
- FLOATING: don't care or floating around  $V_{REF}$
- Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.
- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting.  
RON =  $RZQ/7$  (34  $\Omega$  in MR1);  
Qoff = 0 (Output Buffer enabled in MR1);  
RTT\_Nom =  $RZQ/6$  (40  $\Omega$  in MR1);  
RTT\_WR =  $RZQ/2$  (120  $\Omega$  in MR2)  
TDQS Feature disabled in MR1
- Define D = {/CS, /RAS, /CAS, /WE} : = {H, L, L, L}
- Define /D = {/CS, /RAS, /CAS, /WE} : = {H, H, H, H}

Note: The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.



### Measurement Setup and Test Load for IDD and IDDQ Measurements



### Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement.

[Timings used for IDD and IDDQ Measurement-Loop Patterns]

Parameter	DDR3-1866	DDR3-1600	DDR3-1333	Unit
	13-13-13	11-11-11	9-9-9	
CL	13	11	9	nCK
tCK (min.)	1.07	1.25	1.5	ns
nRCD (min.)	13	11	9	nCK
nRC (min.)	45	39	33	nCK
nRAS (min.)	32	28	24	nCK
nRP (min.)	13	11	9	nCK
nFAW (x8)	26	24	20	nCK
nFAW (x16)	33	32	30	nCK
nRRD (x8)	5	5	4	nCK
nRRD (x16)	6	6	5	nCK
nRFC	103	88	74	nCK

[Basic IDD and IDDQ Measurement Conditions]

Parameter	Symbol	Description
Operating one bank active precharge current	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to IDD0 Measurement-Loop Pattern table; Data I/O: FLOATING; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD0 Measurement-Loop Pattern table); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see IDD0 Measurement-Loop Pattern table
Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1.6; AL: 0; /CS: H between ACT, READ and PRE; Command, address, bank address inputs, data I/O: partially toggling according to IDD1 Measurement-Loop Pattern table; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD1 Measurement-Loop Pattern table); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see IDD1 Measurement-Loop Pattern table
Precharge standby current	IDD2N	CKE: H; External clock: on; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop patterns table BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to IDD2N and IDD3N Measurement-Loop Pattern table; data I/O: FLOATING; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see IDD2N and IDD3N Measurement-Loop Pattern table
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to IDD2NT and IDDQ2NT Measurement-Loop Pattern table; data I/O: FLOATING; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to IDD2NT and IDDQ2NT Measurement-Loop pattern table; pattern details: see IDD2NT and IDDQ2NT Measurement-Loop Pattern table
Precharge power-down current slow exit	IDD2PO	CKE: L; External clock: on; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: FLOATING; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*2; ODT signal: stable at 0; precharge power down mode: slow exit*3
Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: FLOATING; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: FLOATING; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to IDD2N and IDD3N Measurement-Loop Pattern; data I/O: FLOATING; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see IDD2N and IDD3N Measurement-Loop Pattern table
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: FLOATING; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0

Parameter	Symbol	Description
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8 <sup>*1, 6</sup> ; AL: 0; /CS: H between READ; Command, address, bank address Inputs: partially toggling according to IDD4R and IDDQ4R Measurement-Loop Pattern table; data I/O: seamless read data burst with different data between one burst and the next one according to IDD4R and IDDQ4R Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, READ commands cycling through banks: 0,0,1,1,2,2,... (see IDD4R and IDDQ4R Measurement-Loop Pattern table); Output buffer and RTT: enabled in MR <sup>*2</sup> ; ODT signal: stable at 0; pattern details: see IDD4R and IDDQ4R Measurement-Loop Pattern table
Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8 <sup>*1</sup> ; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to IDD4W Measurement-Loop Pattern table; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD4W Measurement-Loop Pattern table); Output buffer and RTT: enabled in MR <sup>*2</sup> ; ODT signal: stable at H; pattern details: see IDD4W Measurement-Loop Pattern table
Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8 <sup>*1</sup> ; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to IDD5B Measurement-Loop Pattern table; data I/O: FLOATING; DM: stable at 0; bank activity: REF command every nRFC (IDD5B Measurement-Loop Pattern); output buffer and RTT: enabled in MR <sup>*2</sup> ; ODT signal: stable at 0; pattern details: see IDD5B Measurement-Loop Pattern table
Self-refresh current: normal temperature range	IDD6	TC: 0 to 85°C; ASR: disabled <sup>*4</sup> ; SRT: Normal <sup>*5</sup> ; CKE: L; External clock: off; CK and /CK: L; CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8 <sup>*1</sup> ; AL: 0; /CS, command, address, bank address, data I/O: FLOATING; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR <sup>*2</sup> ; ODT signal: FLOATING
Self-refresh current: extended temperature range	IDD6E	TC: 0 to 95°C; ASR: Disabled <sup>*4</sup> ; SRT: Extended <sup>*5</sup> ; CKE: L; External clock: off; CK and /CK: L; CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8 <sup>*1</sup> ; AL: 0; /CS, command, address, bank address, data I/O: FLOATING; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR <sup>*2</sup> ; ODT signal: FLOATIN
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Timings used for IDD and IDDQ Measurement-Loop Patterns table; BL: 8 <sup>*1, 6</sup> ; AL: CL-1; /CS: H between ACT and READA; Command, address, bank address Inputs: partially toggling according to IDD7 Measurement-Loop Pattern table; data I/O: read data bursts with different data between one burst and the next one according to IDD7 Measurement-Loop Pattern table; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD7 Measurement-Loop Pattern table; output buffer and RTT: enabled in MR <sup>*2</sup> ; ODT signal: stable at 0; pattern details: see IDD7 Measurement-Loop Pattern table
RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

## Notes:

- Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].
- MR: Mode Register  
Output buffer enable: set MR1 bit A12 = 0 and MR1 bits [5, 1] = [0,1];  
RTT\_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT\_WR enable: set MR2 bits [10, 9] = [1,0].
- Precharge power down mode: set MR0 bit A12 = 0 for Slow Exit or MR0 bit A12 = 1 for fast exit.
- Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.
- Self-refresh temperature range (SRT): set MR2 bit A7 = 0 for normal or 1 for extended temperature range.
- Read burst type: nibble sequential, set MR0 bit A3 = 0.



#### [IDD0 Measurement-Loop Pattern]

CK, /CK	CKE	Sub- Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data*2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	-
			3,4	/D,/D	1	1	1	1	0	0	0	0	0	0	0	-
			...	Repeat pattern 1...4 until nRAS -1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1...4 until nRC -1, truncate if necessary												
			1 x nRC+ 0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			1 x nRC+ 1, 2	D,D	1	0	0	0	0	0	0	0	0	F	0	-
			1 x nRC+ 3, 4	/D,/D	1	1	1	1	0	0	0	0	0	F	0	-
			...	Repeat pattern nRC+1...4 until 1xnRC+nRAS-1, truncate if necessary												
			1xnRC+nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	-
			...	Repeat nRC+1...4 until 2xnRC -1, truncate if necessary												
		1	2 x nRC	nRC Repeat Sub-Loop 0, use BA = 1 instead												
		2	4 x nRC	nRC Repeat Sub-Loop 0, use BA = 2 instead												
		3	6 x nRC	nRC Repeat Sub-Loop 0, use BA = 3 instead												
		4	8 x nRC	nRC Repeat Sub-Loop 0, use BA = 4 instead												
		5	10 x nRC	nRC Repeat Sub-Loop 0, use BA = 5 instead												
		6	12 x nRC	nRC Repeat Sub-Loop 0, use BA = 6 instead												
		7	14 x nRC	nRC Repeat Sub-Loop 0, use BA = 7 instead												

Notes:

1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means the Most Significant Bit (MSB) of Row address.

#### [IDD1 Measurement-Loop Pattern]

CK, /CK	CKE	Sub- Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	-
			3,4	/D,/D	1	1	1	1	0	0	0	0	0	0	0	-
			...	Repeat pattern 1...4 until nRCD -1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			...	Repeat pattern 1...4 until nRAS -1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1...4 until nRC -1, truncate if necessary												
			1 x nRC+ 0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			1 x nRC+ 1, 2	D,D	1	0	0	0	0	0	0	0	0	F	0	-
			1 x nRC+ 3, 4	/D,/D	1	1	1	1	0	0	0	0	0	F	0	-
			...	Repeat pattern nRC+1...4 until nRC+nRCD -1, truncate if necessary												
			1xnRC+nRCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			...	Repeat pattern nRC+1...4 until nRC+nRAS -1, truncate if necessary												
			1 x nRC+ nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	-
			...	Repeat pattern nRC+1...4 until 2xnRC -1, truncate if necessary												
		1	2 x nRC	nRC Repeat Sub-Loop 0, use BA = 1 instead												
		2	4 x nRC	nRC Repeat Sub-Loop 0, use BA = 2 instead												
		3	6 x nRC	nRC Repeat Sub-Loop 0, use BA = 3 instead												
		4	8 x nRC	nRC Repeat Sub-Loop 0, use BA = 4 instead												
		5	10 x nRC	nRC Repeat Sub-Loop 0, use BA = 5 instead												
		6	12 x nRC	nRC Repeat Sub-Loop 0, use BA = 6 instead												
		7	14 x nRC	nRC Repeat Sub-Loop 0, use BA = 7 instead												

Notes:

1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ Signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

#### [IDD2N and IDD3N Measurement-Loop Pattern]

CK, /CK	CKE	Sub -Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	/D	1	1	1	1	0	0	0	0	0	F	0	-
			3	/D	1	1	1	1	0	0	0	0	0	F	0	-
		1	4 to 7	Repeat Sub-Loop 0, use BA= 1 instead												
		2	8 to 11	Repeat Sub-Loop 0, use BA= 2 instead												
		3	12 to 15	Repeat Sub-Loop 0, use BA= 3 instead												
		4	16 to 19	Repeat Sub-Loop 0, use BA= 4 instead												
		5	20 to 23	Repeat Sub-Loop 0, use BA= 5 instead												
		6	24 to 27	Repeat Sub-Loop 0, use BA= 6 instead												
		7	28 to 31	Repeat Sub-Loop 0, use BA= 7 instead												

#### Notes:

1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ Signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

#### [IDD2NT Measurement-Loop Pattern]

CK, /CK	CKE	Sub -Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	/D	1	1	1	1	0	0	0	0	0	F	0	-
			3	/D	1	1	1	1	0	0	0	0	0	F	0	-
		1	4 to 7	Repeat Sub-Loop 0, but ODT = 0 and BA= 1												
		2	8 to 11	Repeat Sub-Loop 0, but ODT = 1 and BA= 2												
		3	12 to 15	Repeat Sub-Loop 0, but ODT = 1 and BA= 3												
		4	16 to 19	Repeat Sub-Loop 0, but ODT = 0 and BA= 4												
		5	20 to 23	Repeat Sub-Loop 0, but ODT = 0 and BA= 5												
		6	24 to 27	Repeat Sub-Loop 0, but ODT = 1 and BA= 6												
		7	28 to 31	Repeat Sub-Loop 0, but ODT = 1 and BA= 7												

#### Notes:

1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ Signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address

#### [IDD4R and IDDQ4R Measurement-Loop Pattern]

CK, /CK	CKE	Sub -Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2, 3	/D, /D	1	1	1	1	0	0	0	0	0	0	0	-
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	-
			6, 7	/D, /D	1	1	1	1	0	0	0	0	0	F	0	-
		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 64	Repeat Sub-Loop 0, but BA= 7												

#### Notes:

1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ Signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

**[IDD4W Measurement-Loop Pattern]**

CK, /CK	CKE	Sub -Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	-
			2, 3	/D, /D	1	1	1	1	1	0	0	0	0	0	0	-
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	-
			6, 7	/D, /D	1	1	1	1	1	0	0	0	0	F	0	-
		1	8 to 15	Repeat Sub-Loop 0, but BA = 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA = 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA = 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA = 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA = 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA = 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA = 7												

Notes:

1. DM must be driven low all the time. DQS, /DQS are used according to write commands, otherwise MID-LEVEL.
2. Burst sequence driven on each DQ signal by write command. Outside burst operation, DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means the Most Significant Bit (MSB) of Row address.

**[IDD5B Measurement-Loop Pattern]**

CK, /CK	CKE	Sub -Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	-
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	-
			5 to 8	Repeat cycles 1..4 but BA = 1												
			9 to 12	Repeat cycles 1..4 but BA = 2												
			13 to 16	Repeat cycles 1..4 but BA = 3												
			17 to 20	Repeat cycles 1..4 but BA = 4												
			21 to 24	Repeat cycles 1..4 but BA = 5												
			25 to 28	Repeat cycles 1..4 but BA = 6												
			29 to 32	Repeat cycles 1..4 but BA = 7												
		2	33 to nRFC - 1	Repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

Notes:

1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
2. DQ signals are MID-LEVEL.
3. BA: BA0 to BA2.
4. Am: m means the Most Significant Bit (MSB) of Row address.

[IDD7 Measurement-Loop Pattern]

CK, /CK	CKE	Sub -Loop	Cycle Number	Com -mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data *2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat above D Command until nRRD-1												
		1	nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	-
			...	Repeat above D Command until 2 x nRRD- 1												
		2	2 x nRRD	Repeat Sub-Loop 0, but BA = 2												
		3	3 x nRRD	Repeat Sub-Loop 1, but BA = 3												
		4	4 x nRRD	D	1	0	0	0	0	3	0	0	0	F	0	-
				Assert and repeat above D Command until nFAW- 1, if necessary												
		5	nFAW	Repeat Sub-Loop 0, but BA = 4												
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BA = 5												
		7	nFAW + 2 x nRRD	Repeat Sub-Loop 0, but BA = 6												
		8	nFAW + 3 x nRRD	Repeat Sub-Loop 1, but BA = 7												
		9	nFAW + 4 x nRRD	D	1	0	0	0	0	7	0	0	0	F	0	-
				Assert and repeat above D Command until 2 x nFAW- 1, if necessary												
		10	2 x nFAW +0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			2 x nFAW +1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 x nFAW	D	1	0	0	0	0	0	0	0	0	F	0	-
			+2	Repeat above D command until 2 x nFAW + nRRD - 1												
		11	2 x nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	-
			2 x nFAW + nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 x nFAW	D	1	0	0	0	0	1	0	0	0	0	0	-
			+ nRRD + 2	Repeat above D command until 2 x nFAW + 2 x nRRD - 1												
		12	2 x nFAW + 2 x nRRD	Repeat Sub-Loop 10, but BA = 2												
		13	2 x nFAW + 3 x nRRD	Repeat Sub-Loop 11, but BA = 3												
		14	2 x nFAW + 4 x nRRD	D	1	0	0	0	0	3	0	0	0	0	0	-
				Assert and repeat above D command until 3 x nFAW - 1, if necessary												
		15	3 x nFAW	Repeat Sub-Loop 10, but BA = 4												
		16	3 x nFAW + nRRD	Repeat Sub-Loop 11, but BA = 5												
		17	3 x nFAW + 2 x nRRD	Repeat Sub-Loop 10, but BA = 6												
		18	3 x nFAW + 3 x nRRD	Repeat Sub-Loop 11, but BA = 7												
		19	3 x nFAW + 4 x nRRD	D	1	0	0	0	0	7	0	0	0	0	0	-
				Assert and repeat above D command until 4 x nFAW - 1, if necessary												

Notes:

- DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
- Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
- BA: BA0 to BA2.
- Am: m means the Most Significant Bit (MSB) of Row address.

### 5.18.2. IDD and IDDQ Specification

Parameter	Symbol	Data rate (Mbps)	x8 (1.35V)	x8 (1.5V)	x16 (1.35V)	x16 (1.5V)	Unit	Notes
			max.	max.	max.	max.		
Operating current (ACT-PRE)	IDD0	1866	48	48	61	61	mA	
		1600	45	45	58	58		
		1333	43	43	56	56		
Operating current (ACT-READ-PRE)	IDD1	1866	64	64	86	86	mA	
		1600	61	61	82	82		
		1333	58	58	78	78		
Precharge power-down Standby current	IDD2P0	1866	9	9	16	16	mA	Slow PD Exit
		1600	9	9	16	16		
		1333	9	9	16	16		
	IDD2P1	1866	10	10	16	16	mA	Fast PD Exit
		1600	10	10	16	16		
		1333	10	10	16	16		
Precharge quiet standby Current	IDD2Q	1866	27	27	29	29	mA	
		1600	25	25	27	27		
		1333	24	24	27	27		
Precharge standby current	IDD2N	1866	28	28	30	30	mA	
		1600	27	27	29	29		
		1333	25	25	28	28		
Precharge standby current ODT current	IDD2NT	1866	32	32	35	35	mA	
		1600	30	30	33	33		
		1333	28	28	31	31		
Active power-down current (Always fast exit)	IDD3P	1866	24	24	29	29	mA	
		1600	24	24	28	28		
		1333	23	23	28	28		
Active standby current	IDD3N	1866	39	39	43	43	mA	
		1600	36	36	40	40		
		1333	34	34	39	39		
Operating current (Burst read operating)	IDD4R	1866	116	116	172	172	mA	
		1600	103	103	155	155		
		1333	91	91	135	135		
Operating current (Burst write operating)	IDD4W	1866	127	127	196	196	mA	
		1600	112	112	172	172		
		1333	100	100	152	152		
Burst refresh current	IDD5B	1866	160	160	160	160	mA	
		1600	158	158	158	158		
		1333	158	158	158	158		
Self-Refresh current Normal temperature range	IDD6	1866	14	14	20	20	mA	
		1600						
		1333						
Self-Refresh current Extended temperature range	IDD6ET	1866	19	19	27	27	mA	
		1600						
		1333						
All bank interleave read current	IDD7	1866	189	189	258	258	mA	
		1600	174	174	232	232		
		1333	168	168	210	210		
RESET low current	IDD8	1866	Idd2P0+2mA	Idd2P0+2mA	Idd2P0+2mA	Idd2P0+2mA	mA	
		1600						
		1333						

Notes:

- Enabling ASR could increase IDD<sub>x</sub> by up to an additional 2mA.
- The IDD values must be derated (increased) on Industrial and Automotive grade devices when operated outside of the range  $0^{\circ}\text{C} \leq \text{TC} \leq +85^{\circ}\text{C}$ :
  - i. When  $\text{TC} < 0^{\circ}\text{C}$ : IDD2P0, IDD2P1 and IDD3P must be derated by 4%; IDD4R and IDD4W must be derated by 2%; and IDD6, IDD6ET and IDD7 must be derated by 7%.
  - ii. When  $\text{TC} > 85^{\circ}\text{C}$ : IDD0, IDD1, IDD2N, IDD2NT, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, and IDD5B must be derated by 2%; IDD2Px must be derated by 30%.
- For Automotive grade products, when  $\text{TC} > 95^{\circ}\text{C}$ , all IDD excepting IDD6 must be increased by 20%

**5.19. Pin Capacitance( $T_C = 25^\circ\text{C}$ ,  $V_{DD}$ ,  $V_{DDQ} = 1.5\text{V} \pm 0.075\text{V}$ )**

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance	$C_{IO}$	1.4	2.7	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	pF	1, 2
Input capacitance, CK and /CK	$C_{CK}$	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	0.8	1.3	pF	2
Input capacitance delta, CK and /CK	$C_{DCK}$	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	$C_{DDQS}$	0	0.2	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	$C_I$	0.75	1.35	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2, 5
Input capacitance delta, (all control input-only pins)	$C_{DI\_CTRL}$	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2, 6, 7
Input capacitance delta, (all address/command input-only pins)	$C_{DI\_ADD\_CMD}$	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ, DM, DQS, /DQS, TDQS, /TDQS	$C_{DIO}$	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	$C_{ZQ}$	-	3	-	3	-	3	-	3	-	3	pF	2, 11
Output capacitance of /DED pin	$C_{DED}$	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	pF	2

**Notes:**

- Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS
- $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  applied and all other pins floating (excepting the pin under test, CKE, /RESET and ODT as necessary).  
 $V_{DD} = V_{DDQ} = 1.5\text{V}$ ,  $V_{BIAS} = V_{DD}/2$  and on die termination off.
- Absolute value of  $C_{CK}(CK) - C_{CK}(/CK)$
- Absolute value of  $C_{IO}(DQS) - C_{IO}(/DQS)$
- $C_I$  applies to ODT, /CS, CKE, A0-A15, BA0-BA2, /RAS, /CAS and /WE
- $C_{DI\_CTRL}$  applies to ODT, /CS and CKE.
- $C_{DI\_CTRL} = C_I(CTRL) - 0.5 \times (C_I(CK) + C_I(/CK))$
- $C_{DI\_ADD\_CMD}$  applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE
- $C_{DI\_ADD\_CMD} = C_I(ADD\_CMD) - 0.5 \times (C_I(CK) + C_I(/CK))$
- $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS) + C_{IO}(/DQS))$
- Maximum external load capacitance on ZQ pin: 5pF

5.20. Pin Capacitance( $T_C = 25^\circ\text{C}$ ,  $V_{DD}$ ,  $V_{DDQ} = 1.35\text{V}$ )

Parameter	Symbol	DDR3L-1600		DDR3L-1866		DDR3L-2133		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input capacitance, CK and /CK	$C_{CK}$	0.8	1.4	0.8	1.3	0.8	1.3	pF	2
Input capacitance delta, CK and /CK	$C_{DCK}$	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance	$C_{IO}$	1.4	2.2	1.4	2.1	1.4	2.1	pF	1, 2
Input/output capacitance delta, DQS and /DQS	$C_{DDQS}$	0	0.15	0	0.15	0	0.15	pF	2, 4
Input/output capacitance delta, DQ, DM, DQS, /DQS, TDQS, /TDQS	$C_{DIO}$	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 10
Input capacitance, (control, address, command, input-only pins)	$C_i$	0.75	1.2	0.75	1.2	0.75	1.2	pF	2, 5
Input capacitance delta, (all control input-only pins)	$C_{DI\_CTRL}$	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2, 6, 7
Input capacitance delta, (all address/command input-only pins)	$C_{DI\_ADD\_CMD}$	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 8, 9
ZQ pin capacitance	$C_{ZQ}$	-	3.0	-	3.0	-	3.0	pF	2
Reset pin capacitance	$C_{RE}$	-	3.0	-	3.0	-	3.0	pF	
Output capacitance of /DED pin	$C_{DED}$	-	2.5	-	2.5	-	2.5	pF	2

Notes:

- Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS
- $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  applied and all other pins floating (excepting the pin under test, CKE, /RESET and ODT as necessary).  
 $V_{DD} = V_{DDQ} = 1.35\text{V}$ ,  $V_{BIAS} = V_{DD}/2$  and on die termination off.
- Absolute value of  $C_{CK}(CK) - C_{CK}(/CK)$
- Absolute value of  $C_{IO}(DQS) - C_{IO}(/DQS)$
- $C_i$  applies to ODT, /CS, CKE, A0-A15, BA0-BA2, /RAS, /CAS and /WE
- $C_{DI\_CTRL}$  applies to ODT, /CS and CKE.
- $C_{DI\_CTRL} = C_i(CTRL) - 0.5 \times (C_i(CK) + C_i(/CK))$
- $C_{DI\_ADD\_CMD}$  applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE
- $C_{DI\_ADD\_CMD} = C_i(ADD\_CMD) - 0.5 \times (C_i(CK) + C_i(/CK))$
- $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS) + C_{IO}(/DQS))$



### 5.21. Standard Speed Bins

Speed Bin			DDR3-1333		DDR3-1600		DDR3-1866		Unit
CL-nRCD-nRP			9-9-9		11-11-11		13-13-13		
Parameter	Symobl		min.	max.	min.	max.	min.	max.	
Internal read command to first data	tAA	13.5 (13.125)*	20.0		13.75 (13.125)*	20.0	13.91 (13.125)*	20.0	ns
ACT to internal read or write delay time	tRCD	13.5 (13.125)*					13.75 (13.125)*		-
PRE command period	tRP	13.5 (13.125)*	-		13.75 (13.125)*	-	13.91 (13.125)*	-	ns
ACT to ACT or REF command period	tRC	49.5 (49.125)*	-		48.75 (48.125)*	-	47.91 (47.125)*	-	ns
ACT to PRE command period	tRAS	36	9 x tREFI		35	9 x tREFI	34	9 x tREFI	ns
CL=5	CWL = 5	tCK (avg)	3.0	3.3	3.0	3.3	3.0	3.3	ns
	CWL = 6, 7, 8, 9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=6	CWL = 5	tCK (avg)	2.5	3.3	2.5	3.3	2.5	3.3	ns
	CWL = 6	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL = 7, 8, 9	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=7	CWL = 5	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL = 6	tCK (avg)	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns
	CWL = 7, 8, 9, 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=8	CWL = 5	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL = 6	tCK (avg)	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns
	CWL = 7, 8, 9, 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=9	CWL = 5, 6	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL = 7	tCK (avg)	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns
	CWL = 8, 9, 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=10	CWL = 5, 6	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL = 7	tCK (avg)	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns
	CWL = 8, 9, 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=11	CWL = 5, 6, 7	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL= 8	tCK (avg)	Reserved		1.25	<1.5	1.25	<1.5	ns
	CWL= 9, 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=12	CWL= 5, 6, 7, 8, 9, 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=13	CWL = 5, 6, 7, 8	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL= 9	tCK (avg)	Reserved		Reserved		1.07	<1.25	ns
	CWL= 10	tCK (avg)	Reserved		Reserved		Reserved		ns
CL=14	CWL= 5, 6, 7, 8, 9	tCK (avg)	Reserved		Reserved		Reserved		ns
	CWL= 10	tCK (avg)	Reserved		Reserved		Reserved		ns
Supported CL settings			5, 6, 7, 8, 9, 10		5, 6, 7, 8, 9, 10, 11		5, 6, 7, 8, 9, 10, 11, 13		nCK
Supported CWL settings			5, 6, 7		5, 6, 7, 8		5, 6, 7, 8, 9		nCK

#### Note:

- For devices supporting optional down binning to CL=7 and CL=9, tAA/tRCD/tRPmin must be 13.125 ns. SPD settings must be programmed to match. For example, DDR3-1333 devices supporting down binning to DDR3-1066 should program 13.125 ns in SPD bytes for tAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600 devices supporting down binning to DDR3-1333 or DDR3-1066 should program 13.125 ns in SPD bytes for tAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333 and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600.

5.22. DDR3 AC Characteristics (TC = 25°C, VDD, VDDQ = 1.5V ± 0.075V)

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
Clock Timing							
Average clock period	tCK(avg)	min	1500	1250	1070	ps	40
		max	3333			ps	
Minimum clock cycle time	tCK(DLL-off)	min	8			ns	6
Average High pulse width	tCH(avg)	min	0.47			tCK(avg)	42
		max	0.53				
Average Low pulse width	tCL(avg)	min	0.47			tCK(avg)	43
		max	0.53				
Absolute clock period	tCK(abs)	min	t <sub>CK</sub> (avg)min + t <sub>JIT</sub> (per)min			ns	41
		max	t <sub>CK</sub> (avg)max + t <sub>JIT</sub> (per)max			ns	
Absolute High clock pulse width	tCH(abs)	min	0.43			tCK(avg)	38
Absolute Low clock pulse width	tCL(abs)	min	0.43			tCK(avg)	39
Command and Address Timing Parameters							
Active to read/write	tRCD	min	see speed bins table			ns	
Precharge command period	tRP	min	see speed bins table			ns	
Active to active/auto-refresh	tRC	min	see speed bins table			ns	
Active to precharge	tRAS	min	see speed bins table			ns	
		max	see speed bins table			ns	
Control and Address input pulse width for each input	tIPW	min	620	560	535	ps	32
Active bank A to Active bank B (x8)	tRRD (x8)	min	max(4nCK, 6ns)		max(4nCK, 5ns)	-	26,27
Active bank A to Active bank B (x16)	tRRD (x16)	min	max(4nCK, 7.5ns)		max(4nCK, 6ns)	-	26,27
Four active window (x8)	tFAW (x8)	min	30	30	27	ns	26
Four active window (x16)	tFAW (x16)	min	45	40	35	ns	26
Address and control input hold time (VIH/VIL (DC100) levels; SR=1V/ns)	tIH(base) DC100	min	140	120	100	ps	16,23
Address and control input setup time (VIH/VIL (AC175) levels; SR=1V/ns)	tIS(base) AC175	min	65	45	-	ps	16,23
Address and control input setup time (VIH/VIL (AC150) levels; SR=1V/ns)	tIS(base) AC150	min	190	170	-	ps	16,23,31
Address and control input setup time (VIH/VIL (AC125) levels; SR=1V/ns)	tIS(base) AC125	min	-	-	150	ps	16,23
/CAS to /CAS command delay	tCCD	min	4			nCK	
Mode register set command cycle time	tMRD	min	4			nCK	
Mode register set command update delay	tMOD	min	max(12nCK, 15ns)			-	27
Write recovery time	tWR	min	15			ns	26
Auto precharge write recovery + precharge time	tDAL	min	WR + RU (tRP/tCK(avg))			nCK	
Multi-Purpose register Recovery time	tMPRR	min	1			nCK	28
Internal write to read command delay	tWTR	min	max(4nCK, 7.5ns)			-	18,26,27
Internal read to precharge command delay	tRTP	min	max(4nCK, 7.5ns)			-	26,27
Exit reset from CKE high to a valid command	tXPR	min	max(5nCK, tRFC(min))+10ns)			-	27
DLL locking time	tDLLK	min	512			nCK	

Parameter	Symbol	min/max	Data Rate			Unit	
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
DQ input Parameters							
DQ and DM input hold time (VIH/VIL (DC100) levels)	tDH(base) DC100 SR=1V/ns	min	65	45	-	ps	17,25
DQ and DM input hold time (VIH/VIL (DC100) levels)	tDH(base) DC100 SR=2V/ns	min	-	-	70	ps	17,25
Q and DM input hold time (VIH/VIL (AC150) levels)	DS(base) AC150 SR=1V/ns	min	30	10	-	ps	17,25
DQ and DM input hold time (VIH/VIL (AC135) levels)	tDS(base) AC135 SR=1V/ns	min	60	40	-	ps	17,25
DQ and DM input hold time (VIH/VIL (AC135) levels)	tDS(base) AC135 SR=2V/ns	min	-	-	68	ps	17,25
DQ and DM input pulsen width for each	tDIPW	min	400	360	320	ps	32
DQ output Parameters							
DQS, /DQS to DQ skew, per group, per access	tDQSQ	max	125	100	85	ps	12,13
DQ output hold time from DQS, /DQS	tQH	min	0.38			tCK(avg)	12,13,37
DQ high-impedance time	tHZ(DQ)	max	250	225	195	ps	12,13,14,36
DQ low-impedance time	tLZ(DQ)	min	-500	-450	-390	ps	12,13,14,36
		max	250	225	195	ps	
DQ strobe input Parameters							
DQS latching rising transitions to associated clock edge	tDQSS	min	-0.25	-0.27		tCK(avg)	24
		max	0.25	0.27		tCK(avg)	
DQS input high pulse width	tDQSH	min	0.45			tCK(avg)	33,34
		max	0.55			tCK(avg)	
DQS input low pulse width	tDQSL	min	0.45			tCK(avg)	33,34
		max	0.55			tCK(avg)	
DQS falling edge hold time from rising CK	tDSH	min	0.2	0.18		tCK(avg)	24,35
DQS falling edge setup time from rising CK	tDSS	min	0.2	0.18		tCK(avg)	24,35
Write preamble	tWPRE	min	0.9			tCK(avg)	1
Write postamble	tWPST	min	0.3			tCK(avg)	1
DQ s strobe output Parameters							
DQS, /DQS ri s ing edge output access time from rising CK, /CK	tDQSCK	min	-255	-225	-195	ps	12,13,36
		max	255	225	195	ps	
DQS output high time	tQSH	min	0.4			tCK(avg)	12,13,37
DQS output low ti me	tQSL	min	0.4			tCK(avg)	12,13,37
DQS, /DQS high-impedance time (RL + BL/2 reference)	tHZ(DQS)	max	250	225	195	ps	12,13,14,36
DQS, /DQS high-impedance time (RL + BL/2 reference)	tLZ(DQS)	min	-500	-450	-390	ps	12,13,14,36
		max	250	225	195	ps	
Read preamble	tRPRE	min	0.9			tCK(avg)	13,19,37
Read postamble	tRPST	min	0.3			tCK(avg)	13,19,37

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
Power-down Entry Parameters							
Timing of ACT command to power-down entry	tACTPDEN	min	1			nCK	20
Timing of Precharge/Precharge ALL command to power-down entry	tPRPDEN	min	1			nCK	20
Timing of Read/Read with auto-precharge command to power-down entry	tRDPDEN	min	RL + 4 + 1			nCK	
Timing of Write command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	min	WL + 4 + tWR/tCK(avg)			nCK	9
Timing of Write command to power-down entry (BC4MRS)		min	WL + 2 + tWR/tCK(avg)			nCK	9
Timing of Write with auto-precharge command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	min	WL + 4 + WR + 1			nCK	10
Timing of Write with auto-precharge command to power-down entry (BC4MRS)		min	WL + 2 + WR + 1			nCK	10
Timing of REF command to power-down entry	tREFPDEN	min	1			nCK	20,21
Timing of MRS command to power-down entry	tMRSPDEN	min	tMOD(min)			-	
Exit precharge power-down with DLL frozen to command requiring a locked DLL	tXPDLL	min	max(10nCK, 24ns)			-	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	tXP	min	max(3nCK, 6ns)			-	27
CKE minimum pulse width (high and low pulse width)	tCKE	min	max(3nCK, 5.625ns)	max(3nCK, 5ns)		-	27
Power-down entry to exit timing	tPD	min	tCKE(min)			-	15
		max	9 x tREFI			-	
Command pass disable delay	tCPDED	min	1		2	nCK	
ODT to power-down entry/exit latency	tANPD	min	WL - 1			-	
Refresh Parameters							
Auto-refresh to Active/auto-refresh command time	tRFC	min	260			ns	
Average periodic refresh interval (TC ≤ +85°C)	tREFI	max	7.8			μs	
Average periodic refresh interval (TC > +85°C)			3.9			μs	
Minimum CKE low width for self-refresh entry to exit timing	tCKESR	min	tCKE(min) + 1nCK			-	
Valid clock requirement after self-refresh entry or power-down entry	tCKSRE	min	max(5nCK, 10ns)			-	27
Valid clock requirement before self-refresh exit or power-down exit	tCKSRX	min	max(5nCK, 10ns)			-	27
Exit self-refresh to commands not requiring a locked DLL	tXS	min	max(5nCK, tRFC(min) + 10ns)			-	27
Exit self-refresh to commands requiring a locked DLL	tXSDLL	min	tDLLK(min)			nCK	2

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
ODT Timing Parameters							
RTT turn-on	tAON	min	-250	-225	-195	ps	7,12,36
		max	250	225	195	ps	
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	tAONPD	min	2			ns	
		max	8.5			ns	
RTT_Nom and RTT_WR turn-off Time from ODTLoff reference	tAOF	min	0.3			tCK(avg)	8,12,36
		max	0.7			tCK(avg)	
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	tAOFPD	min	2			ns	
		max	8.5			ns	
ODT turn-on latency	ODTLon	-	WL - 2			nCK	
ODT turn-off latency	ODTLoff	-	WL - 2			nCK	
ODT latency for changing from RTT_Nom to RTT_WR	ODTLcnw	-	WL - 2			nCK	
ODT latency for changing from RTT_WR to RTT_Nom(BC4)	ODTLcnw4	-	4 + ODTLoff			nCK	
ODT latency for changing from RTT_WR to RTT_Nom(BL8)	ODTLcnw8	-	6 + ODTLoff			nCK	
Minimum ODT high time after ODT assertion or agter Write (BL4)	ODTH4	min	4			nCK	
Minimum ODT high time after Write (BL8)	ODTH8	min	6			nCK	
RTT change skew	tADC	min	0.3			tCK(avg)	12,36
		max	0.7			tCK(avg)	
Calibration Timing Parameters							
Power-up and rest calibration time	tZQinit	min	max(512nCK, 640ns)			-	
Normal operation full calibratio time	tZQoper	min	max(256nCK, 320ns)			-	
Normal operation short calibratio time	tZQCS	min	max(64nCK, 80ns)			-	29
Write leveling Timing Parameters							
First DQS pulse rising edge after write leveling mode is programmed	tWLMRD	min	40			nCK	3
DQS, /DQS delay after write leveling mode is programmed	tWLDQSEN	min	25			nCK	3
Write leveling setup time from rising CK, /CK crossing to rising DQS, /DQS crossing	tWLS	min	195	165	140	ps	
Write leveling setup time from rising DQS, /DQS crossing to rising CK, /CK crossing	tWLH	min	195	165	140	ps	
write leveling output delay	tWLO	min	0			ns	
		max	9	7.5		ns	
Write leveling output error	tWLOE	min	0			ns	
		max	2			ns	

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
Clock Jitter Specification							
Clock Period Jitter	t <sub>JIT(per)</sub>	min	-80	-70	-60	ps	45
		max	80	70	60		
Maximum Clock Jitter between two consecutive cycles	t <sub>JIT(cc)</sub>	max	160	140	120	ps	46
Duty cycle Jitter (with allowed jitter)	t <sub>JIT(duty)</sub>	min	-			ps	44
		max	-				
Cumulative error across 2 cycles	t <sub>ERR(2per)</sub>	min	-118	-103	-88	ps	47
		max	118	103	88		
Cumulative error across 3 cycles	t <sub>ERR(3per)</sub>	min	-140	-122	-105	ps	47
		max	140	122	105		
Cumulative error across 4 cycles	t <sub>ERR(4per)</sub>	min	-155	-136	-117	ps	47
		max	155	136	117		
Cumulative error across 5 cycles	t <sub>ERR(5per)</sub>	min	-168	-147	-126	ps	47
		max	168	147	126		
Cumulative error across 6 cycles	t <sub>ERR(6per)</sub>	min	-177	-155	-133	ps	47
		max	177	155	133		
Cumulative error across 7 cycles	t <sub>ERR(7per)</sub>	min	-186	-163	-139	ps	47
		max	186	163	139		
Cumulative error across 8 cycles	t <sub>ERR(8per)</sub>	min	-193	-169	-145	ps	47
		max	193	169	145		
Cumulative error across 9 cycles	t <sub>ERR(9per)</sub>	min	-200	-175	-150	ps	47
		max	200	175	150		
Cumulative error across 10 cycles	t <sub>ERR(10per)</sub>	min	-205	-180	-154	ps	47
		max	205	180	154		
Cumulative error across 11 cycles	t <sub>ERR(11per)</sub>	min	-210	-184	-158	ps	47
		max	210	184	158		
Cumulative error across 12 cycles	t <sub>ERR(12per)</sub>	min	-215	-188	-161	ps	47
		max	215	188	161		
Cumulative error across n = 13, 14 ... 49, 50 cycles	t <sub>ERR(nper)</sub>	min	t <sub>ERR(nper)</sub> min. = (1 + 0.68ln(n)) x t <sub>JIT(per)</sub> min.			ps	48
		max	t <sub>ERR(nper)</sub> max. = (1 + 0.68ln(n)) x t <sub>JIT(per)</sub> max.				

## Notes for AC Electrical Characteristics

- Notes: 1. Actual value dependant upon measurement level definitions. See Figure Method for Calculating tWPRE Transitions and Endpoints and see Figure Method for Calculating tWPST Transitions and Endpoints.
2. Commands requiring locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK (min.) plus tQSH (min.) on the left side and tHZ (DQS) (max.) on the right side. See Figure Clock to Data Strobe Relationship.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (TC).
16. tIS(base) and tIH(base) values are for 1V/ns command/address single-ended slew rate and 2V/ns CK, /CK differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Address/Command Setup, Hold and Derating section.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows:  
For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.  
For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ(DQS)(min.) on the left side and tDQSCK(max.) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, auto precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered low after a refresh command once tREFPDEN(min.) is satisfied, there are cases where additional time such as tXPDLL(min.) is also required. See Figure Power-Down Entry/Exit Clarifications - Case 2.
22.  $t_{JIT}(\text{duty}) = +/ - \{ 0.07 \times t_{CK}(\text{avg}) - [(0.5 - (\min(t_{CH}(\text{avg}), t_{CL}(\text{avg}))) \times t_{CK}(\text{avg})] \}$ .  
For example, if tCH/tCL was 0.48/0.52, tJIT(duty) would calculate out to  $\pm 25\text{ps}$  for DDR3-800.  
The tCH(avg) and tCL(avg) values listed must not be exceeded.
23. These parameters are measured from a command/address signal (CKE, /CS, /RAS, /CAS, /WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
24. These parameters are measured from a data strobe signal ((L/U)DQS, /DQS) crossing to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
25. These parameters are measured from a data signal ((L/U)DM, DQ, etc.) transition edge to its respective data strobe signal ((L/U)DQS, /DQS) crossing.



26. For these parameters, the DDR3 SDRAM device is characterized and verified to support  $t_{nPARAM} [nCK] = RU\{t_{PARAM} [ns] / t_{CK}(avg)\}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK}(avg)\}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which  $t_{RP}=15ns$ , the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK}(avg)\} = 6$ , i.e. as long as the input clock jitter specifications are met, precharge command at  $T_m$  and active command at  $T_m+6$  is valid even if  $(T_m+6 - T_m)$  is less than 15ns due to input clock jitter.
27. These parameters should be the larger of the two values, analog (ns) and number of clocks (nCK).
28. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
29. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature ( $T_{driftrate}$ ) and voltage ( $V_{driftrate}$ ) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\text{ZQ Correction} = \frac{0.5}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

where  $T_{sens} = \max.(dRTTdT, dRONdTM)$  and  $V_{sens} = \max.(dRTTdV, dRONdVM)$  define the SDRAM temperature and voltage sensitivities. For example, if  $T_{sens} = 1.5\%/^{\circ}C$ ,  $V_{sens} = 0.15\%/mV$ ,  $T_{driftrate} = 1^{\circ}C/sec$  and  $V_{driftrate} = 15mV/sec$ , then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

30. The  $tIS(base)$  AC150 specifications are adjusted from the  $tIS(base)$  specification by adding an additional 100ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point  $[(175mV - 150mV)/1V/ns]$ .
31. Pulse width of a input signal is defined as the width between the first crossing of  $V_{REF}(DC)$  and the consecutive crossing of  $V_{REF}(DC)$ .
32.  $tDQSL$  describes the instantaneous differential input low pulse width on  $DQS - /DQS$ , as measured from one falling edge to the next consecutive rising edge.
33.  $tDQSH$  describes the instantaneous differential input high pulse width on  $DQS - /DQS$ , as measured from one rising edge to the next consecutive falling edge.
34.  $tDQSH,act + tDQSL,act = 1t_{CK,act}$ ; with  $t_{XYZ,act}$  being the actual measured value of the respective timing parameter in the application.
35.  $tDSH,act + tDSS,act = 1t_{CK,act}$ ; with  $t_{XYZ,act}$  being the actual measured value of the respective timing parameter in the application.
36. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $tERR(mper),act$  of the input clock, where  $2 \leq m \leq 12$ . (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has  $tERR(mper),act,min = -172ps$  and  $tERR(mper),act,max = +193ps$ , then  $tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = -400ps - 193ps = -593ps$  and  $tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400ps + 172ps = +572ps$ . Similarly,  $tLZ(DQ)$  for DDR3-800 derates to  $tLZ(DQ),min(derated) = -800ps - 193ps = -993ps$  and  $tLZ(DQ),max(derated) = 400ps + 172ps = +572ps$ . Note that  $tERR(mper),act,min$  is the minimum measured value of  $tERR(nper)$  where  $2 \leq n \leq 12$ , and  $tERR(mper),act,max$  is the maximum measured value of  $tERR(nper)$  where  $2 \leq n \leq 12$ .
37. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $tJIT(per),act$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{CK}(avg),act = 2500ps$ ,  $tJIT(per),act,min = -72ps$  and  $tJIT(per),act,max = +93ps$ , then  $tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 \times t_{CK}(avg),act + tJIT(per),act,min = 0.9 \times 2500ps - 72ps = +2178ps$ . Similarly,  $tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 \times t_{CK}(avg),act + tJIT(per),act,min = 0.38 \times 2500ps - 72ps = +878ps$ .



38. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
39. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
40. tCK (avg) is calculated as the average clock period across any consecutive 200cycle window, where each clock period is calculated from rising edge to rising edge.

$$\left( \sum_{j=1}^N tCK_j \right) / N$$

N = 200

41. tCK (abs) is the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK (abs) is not subject to production test.
42. tCH (avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulse.

$$\left( \sum_{j=1}^N tCH_j \right) / (N * tCK_{(avg)})$$

N = 200

43. tCL (avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$\left( \sum_{j=1}^N tCL_j \right) / (N * tCK_{(avg)})$$

N = 200

44. tJIT (duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH (avg). tCL jitter is the largest deviation of any single tCL from tCL (avg). tJIT (duty) is not subject to production test.

tJIT (duty) = Min./Max. of {tJIT (CH), tJIT (CL)}, where:

tJIT (CH) = {tCH<sub>j</sub> - tCH (avg) where j = 1 to 200}

tJIT (CL) = {tCL<sub>j</sub> - tCL (avg) where j = 1 to 200}

45. tJIT (per) is defined as the largest deviation of any single tCK from tCK (avg).

tJIT (per) = Min./Max. of { tCK<sub>j</sub> - tCK (avg) where j = 1 to 200}

tJIT (per) defines the single period jitter when the DLL is already locked. tJIT (per, lck) uses the same definition for single period jitter, during the DLL locking period only. tJIT (per) and tJIT (per, lck) are not subject to production test.

46. tJIT (cc) is defined as the absolute difference in clock period between two consecutive clock cycles:

tJIT (cc) = Max. of {tCK<sub>j+1</sub> - tCK<sub>j</sub>}

tJIT (cc) defines the cycle when the DLL is already locked. tJIT (cc, lck) uses the same definition for cycle-to-cycle jitter, during the DLL locking period only. tJIT (cc) and tJIT (cc, lck) are not subject to production test.

47. tERR (nper) is defined as the cumulative error across n multiple consecutive cycles from tCK (avg).

tERR (nper) is not subject to production test.

48. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

49. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing hold at all times. (minimum and maximum of spec values are to be used for calculations in the table below.)

Parameter	Symbol	Min.	Max.	Unit
Absolute clock period	tCK (abs)	tCK (avg)min. + tJIT (per)min.	tCK (avg)max. + tJIT (per)max.	ps
Absolute clock high pulse width	tCH (abs)	tCH (avg)min. x tCK (avg)min. + tJIT (duty)min.	tCH (avg)max. x tCK (avg)max. + tJIT (duty)max.	ps
Absolute clock low pulse width	tCL (abs)	tCL (avg)min. x tCK (avg)min. + tJIT (duty)min.	tCL (avg)max. x tCK (avg)max. + tJIT (duty)max.	ps

50. tCH (abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
51. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

5.23. DDR3L AC Characteristics (TC = 25°C, VDD, VDDQ = 1.35V)

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
Clock Timing							
Average clock period	tCK(avg)	min	1500	1250	1070	ps	40
		max	3333			ps	
Minimum clock cycle time	tCK(DLL-off)	min	8			ns	6
Average High pulse width	tCH(avg)	min	0.47			tCK(avg)	42
		max	0.53				
Average Low pulse width	tCL(avg)	min	0.47			tCK(avg)	43
		max	0.53				
Absolute clock period	tCK(abs)	min	t <sub>CK</sub> (avg)min + t <sub>JIT</sub> (per)min			ns	41
		max	t <sub>CK</sub> (avg)max + t <sub>JIT</sub> (per)max			ns	
Absolute High clock pulse width	tCH(abs)	min	0.43			tCK(avg)	38
Absolute Low clock pulse width	tCL(abs)	min	0.43			tCK(avg)	39
Command and Address Timing Parameters							
Active to read/write	tRCD	min	see speed bins table			ns	
Precharge command period	tRP	min	see speed bins table			ns	
Active to active/auto-refresh	tRC	min	see speed bins table			ns	
Active to precharge	tRAS	min	see speed bins table			ns	
		max	see speed bins table			ns	
Control and Address input pulse width for each input	tIPW	min	620	560	535	ps	32
Active bank A to Active bank B (x8)	tRRD (x8)	min	max(4nCK, 6ns)		max(4nCK, 5ns)	-	26,27
Active bank A to Active bank B (x16)	tRRD (x16)	min	max(4nCK, 7.5ns)		max(4nCK, 6ns)	-	26,27
Four active window (x8)	tFAW (x8)	min	30	30	27	ns	26
Four active window (x16)	tFAW (x16)	min	45	40	35	ns	26
Address and control input hold time (VIH/VIL (DC90) levels; SR=1V/ns)	tIH(base) DC90	min	150	130	110	ps	16,23
Address and control input setup time (VIH/VIL (AC160) levels; SR=1V/ns)	tIS(base) AC160	min	80	60	-	ps	16,23
Address and control input setup time (VIH/VIL (AC135) levels; SR=1V/ns)	tIS(base) AC135	min	205	185	65	ps	16,23,31
Address and control input setup time (VIH/VIL (AC125) levels; SR=1V/ns)	tIS(base) AC125	min	-	-	150	ps	16,23
/CAS to /CAS command delay	tCCD	min	4			nCK	
Mode register set command cycle time	tMRD	min	4			nCK	
Mode register set command update delay	tMOD	min	max(12nCK, 15ns)			-	27
Write recovery time	tWR	min	15			ns	26
Auto precharge write recovery + precharge time	tDAL	min	WR + RU (tRP/tCK(avg))			nCK	
Multi-Purpose register Recovery time	tMPRR	min	1			nCK	28
Internal write to read command delay	tWTR	min	max(4nCK, 7.5ns)			-	18,26,27
Internal read to precharge command delay	tRTP	min	max(4nCK, 7.5ns)			-	26,27
Exit reset from CKE high to a valid command	tXPR	min	max(5nCK, tRFC(min))+10ns)			-	27
DLL locking time	tDLLK	min	512			nCK	

Parameter	Symbol	min/max	Data Rate			Unit	
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
DQ input Parameters							
DQ and DM input hold time (VIH/VIL (DC90) levels)	H(base) DC90 SR=1V/ns	min	75	55	-	ps	17,25
DQ and DM input hold time (VIH/VIL (DC90) levels)	H(base) DC90 SR=2V/ns	min	-	-	75	ps	17,25
DQ and DM input hold time (VIH/VIL (AC135) levels)	tDS(base) AC135 SR=1V/ns	min	45	25	-	ps	17,25
DQ and DM input hold time (VIH/VIL (AC130) levels)	tDS(base) AC130 SR=2V/ns	min	-	-	70	ps	17,25
DQ and DM input pulsen width for each	tDIPW	min	400	360	320	ps	32
DQ output Parameters							
DQS, /DQS to DQ skew, per group, per access	tDQSQ	max	125	100	85	ps	12,13
DQ output hold time from DQS, /DQS	tQH	min	0.38			tCK(avg)	12,13,37
DQ high-impedance time	tHZ(DQ)	max	250	225	195	ps	12,13,14,36
DQ low-impedance time	tLZ(DQ)	min	-500	-450	-390	ps	12,13,14,36
		max	250	225	195	ps	
DQ strobe input Parameters							
DQS latching rising transitions to associated clock edge	tDQSS	min	-0.25	-0.27		tCK(avg)	24
		max	0.25	0.27		tCK(avg)	
DQS input high pulse width	tDQSH	min	0.45			tCK(avg)	33,34
		max	0.55			tCK(avg)	
DQS input low pulse width	tDQSL	min	0.45			tCK(avg)	33,34
		max	0.55			tCK(avg)	
DQS falling edge hold time from rising CK	tDSH	min	0.2	0.18		tCK(avg)	24,35
DQS falling edge setup time from rising CK	tDSS	min	0.2	0.18		tCK(avg)	24,35
Write preamble	tWPRE	min	0.9			tCK(avg)	1
Write postamble	tWPST	min	0.3			tCK(avg)	1
DQ s trobe output Parameters							
DQS, /DQS ri s ing edge output access time from rising CK, /CK	tDQSK	min	-255	-225	-195	ps	12,13,36
		max	255	225	195	ps	
DQS output high time	tQSH	min	0.4			tCK(avg)	12,13,37
DQS output low ti me	tQSL	min	0.4			tCK(avg)	12,13,37
DQS, /DQS high-impedance time (RL + BL/2 reference)	tHZ(DQS)	max	250	225	195	ps	12,13,14,36
DQS, /DQS high-impedance time (RL + BL/2 reference)	tLZ(DQS)	min	-500	-450	-390	ps	12,13,14,36
		max	250	225	195	ps	
Read preamble	tRPRE	min	0.9			tCK(avg)	13,19,37
Read postamble	tRPST	min	0.3			tCK(avg)	13,19,37

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
Power-down Entry Parameters							
Timing of ACT command to power-down entry	tACTPDEN	min	1			nCK	20
Timing of Precharge/Precharge ALL command to power-down entry	tPRPDEN	min	1			nCK	20
Timing of Read/Read with auto-precharge command to power-down entry	tRDPDEN	min	RL + 4 + 1			nCK	
Timing of Write command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	min	WL + 4 + tWR/tCK(avg)			nCK	9
Timing of Write command to power-down entry (BC4MRS)		min	WL + 2 + tWR/tCK(avg)			nCK	9
Timing of Write with auto-precharge command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	min	WL + 4 + WR + 1			nCK	10
Timing of Write with auto-precharge command to power-down entry (BC4MRS)		min	WL + 2 + WR + 1			nCK	10
Timing of REF command to power-down entry	tREFPDEN	min	1			nCK	20,21
Timing of MRS command to power-down entry	tMRSPDEN	min	tMOD(min)			-	
Exit precharge power-down with DLL frozen to command requiring a locked DLL	tXPDLL	min	max(10nCK, 24ns)			-	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	tXP	min	max(3nCK, 6ns)			-	27
CKE minimum pulse width (high and low pulse width)	tCKE	min	max(3nCK, 5.625ns)	max(3nCK, 5ns)		-	27
Power-down entry to exit timing	tPD	min	tCKE(min)			-	15
		max	9 x tREFI			-	
Command pass disable delay	tCPDED	min	1		2	nCK	
ODT to power-down entry/exit latency	tANPD	min	WL - 1			-	
Refresh Parameters							
Auto-refresh to Active/auto-refresh command time	tRFC	min	260			ns	
Average periodic refresh interval (TC ≤ +85°C)	tREFI	max	7.8			μs	
Average periodic refresh interval (TC > +85°C)			3.9			μs	
Minimum CKE low width for self-refresh entry to exit timing	tCKESR	min	tCKE(min) + 1nCK			-	
Valid clock requirement after self-refresh entry or power-down entry	tCKSRE	min	max(5nCK, 10ns)			-	27
Valid clock requirement before self-refresh exit or power-down exit	tCKSRX	min	max(5nCK, 10ns)			-	27
Exit self-refresh to commands not requiring a locked DLL	tXS	min	max(5nCK, tRFC(min) + 10ns)			-	27
Exit self-refresh to commands requiring a locked DLL	tXSDLL	min	tDLLK(min)			nCK	2

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
ODT Timing Parameters							
RTT turn-on	tAON	min	-250	-225	-195	ps	7,12,36
		max	250	225	195	ps	
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	tAONPD	min	2			ns	
		max	8.5			ns	
RTT_Nom and RTT_WR turn-off Time from ODTLoff reference	tAOF	min	0.3			tCK(avg)	8,12,36
		max	0.7			tCK(avg)	
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	tAOFPD	min	2			ns	
		max	8.5			ns	
ODT turn-on latency	ODTLon	-	WL - 2			nCK	
ODT turn-off latency	ODTLoff	-	WL - 2			nCK	
ODT latency for changing from RTT_Nom to RTT_WR	ODTLcnw	-	WL - 2			nCK	
ODT latency for changing from RTT_WR to RTT_Nom(BC4)	ODTLcnw4	-	4 + ODTLoff			nCK	
ODT latency for changing from RTT_WR to RTT_Nom(BL8)	ODTLcnw8	-	6 + ODTLoff			nCK	
Minimum ODT high time after ODT assertion or agter Write (BL4)	ODTH4	min	4			nCK	
Minimum ODT high time after Write (BL8)	ODTH8	min	6			nCK	
RTT change skew	tADC	min	0.3			tCK(avg)	12,36
		max	0.7			tCK(avg)	
Calibration Timing Parameters							
Power-up and rest calibration time	tZQinit	min	max(512nCK, 640ns)			-	
Normal operation full calibratio time	tZQoper	min	max(256nCK, 320ns)			-	
Normal operation short calibratio time	tZQCS	min	max(64nCK, 80ns)			-	29
Write leveling Timing Parameters							
First DQS pulse rising edge after write leveling mode is programmed	tWLMRD	min	40			nCK	3
DQS, /DQS delay after write leveling mode is programmed	tWLDQSEN	min	25			nCK	3
Write leveling setup time from rising CK, /CK crossing to rising DQS, /DQS crossing	tWLS	min	195	165	140	ps	
Write leveling setup time from rising DQS, /DQS crossing to rising CK, /CK crossing	tWLH	min	195	165	140	ps	
write leveling output delay	tWLO	min	0			ns	
		max	9	7.5		ns	
Write leveling output error	tWLOE	min	0			ns	
		max	2			ns	

Parameter	Symbol	min/max	Data Rate			Unit	Notes
			1333	1600	1866	MT/s	
Max. Frequency			667	800	933	MHz	
Clock Jitter Specification							
Clock Period Jitter	t <sub>JIT(per)</sub>	min	-80	-70	-60	ps	45
		max	80	70	60		
Maximum Clock Jitter between two consecutive cycles	t <sub>JIT(cc)</sub>	max	160	140	120	ps	46
Duty cycle Jitter (with allowed jitter)	t <sub>JIT(duty)</sub>	min	-			ps	44
		max	-				
Cumulative error across 2 cycles	t <sub>ERR(2per)</sub>	min	-118	-103	-88	ps	47
		max	118	103	88		
Cumulative error across 3 cycles	t <sub>ERR(3per)</sub>	min	-140	-122	-105	ps	47
		max	140	122	105		
Cumulative error across 4 cycles	t <sub>ERR(4per)</sub>	min	-155	-136	-117	ps	47
		max	155	136	117		
Cumulative error across 5 cycles	t <sub>ERR(5per)</sub>	min	-168	-147	-126	ps	47
		max	168	147	126		
Cumulative error across 6 cycles	t <sub>ERR(6per)</sub>	min	-177	-155	-133	ps	47
		max	177	155	133		
Cumulative error across 7 cycles	t <sub>ERR(7per)</sub>	min	-186	-163	-139	ps	47
		max	186	163	139		
Cumulative error across 8 cycles	t <sub>ERR(8per)</sub>	min	-193	-169	-145	ps	47
		max	193	169	145		
Cumulative error across 9 cycles	t <sub>ERR(9per)</sub>	min	-200	-175	-150	ps	47
		max	200	175	150		
Cumulative error across 10 cycles	t <sub>ERR(10per)</sub>	min	-205	-180	-154	ps	47
		max	205	180	154		
Cumulative error across 11 cycles	t <sub>ERR(11per)</sub>	min	-210	-184	-158	ps	47
		max	210	184	158		
Cumulative error across 12 cycles	t <sub>ERR(12per)</sub>	min	-215	-188	-161	ps	47
		max	215	188	161		
Cumulative error across n = 13, 14 ... 49, 50 cycles	t <sub>ERR(nper)</sub>	min	t <sub>ERR(nper)</sub> min. = (1 + 0.68ln(n)) x t <sub>JIT(per)</sub> min.			ps	48
		max	t <sub>ERR(nper)</sub> max. = (1 + 0.68ln(n)) x t <sub>JIT(per)</sub> max.				

## Notes for AC Electrical Characteristics

- Notes: 1. Actual value dependant upon measurement level definitions. See Figure Method for Calculating tWPRE Transitions and Endpoints and see Figure Method for Calculating tWPST Transitions and Endpoints.
2. Commands requiring locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK (min.) plus tQSH (min.) on the left side and tHZ (DQS) (max.) on the right side. See Figure Clock to Data Strobe Relationship.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (TC).
16. tIS(base) and tIH(base) values are for 1V/ns command/address single-ended slew rate and 2V/ns CK, /CK differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Address/Command Setup, Hold and Derating section.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, /DQS differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except /RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows:  
For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.  
For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZ(DQS)(min.) on the left side and tDQSCK(max.) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, auto precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered low after a refresh command once tREFPDEN(min.) is satisfied, there are cases where additional time such as tXPDLL(min.) is also required. See Figure Power-Down Entry/Exit Clarifications - Case 2.
22.  $t_{JIT}(\text{duty}) = +/- \{ 0.07 \times t_{CK}(\text{avg}) - [(0.5 - (\min(t_{CH}(\text{avg}), t_{CL}(\text{avg}))) \times t_{CK}(\text{avg})] \}$ .  
For example, if tCH/tCL was 0.48/0.52, tJIT(duty) would calculate out to +/-125ps for DDR3-800.  
The tCH(avg) and tCL(avg) values listed must not be exceeded.
23. These parameters are measured from a command/address signal (CKE, /CS, /RAS, /CAS, /WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
24. These parameters are measured from a data strobe signal ((L/U)DQS, /DQS) crossing to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
25. These parameters are measured from a data signal ((L/U)DM, DQ, etc.) transition edge to its respective data strobe signal ((L/U)DQS, /DQS) crossing.



26. For these parameters, the DDR3 SDRAM device is characterized and verified to support  $t_{nPARAM} [nCK] = RU\{t_{PARAM} [ns] / t_{CK}(avg)\}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK}(avg)\}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which  $t_{RP}=15ns$ , the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK}(avg)\} = 6$ , i.e. as long as the input clock jitter specifications are met, precharge command at  $T_m$  and active command at  $T_m+6$  is valid even if  $(T_m+6 - T_m)$  is less than 15ns due to input clock jitter.
27. These parameters should be the larger of the two values, analog (ns) and number of clocks (nCK).
28. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
29. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature ( $T_{driftrate}$ ) and voltage ( $V_{driftrate}$ ) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\text{ZQ Correction} = \frac{0.5}{(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

where  $T_{sens} = \max.(dRTTdT, dRONdTM)$  and  $V_{sens} = \max.(dRTTdV, dRONdVM)$  define the SDRAM temperature and voltage sensitivities. For example, if  $T_{sens} = 1.5\%/^{\circ}C$ ,  $V_{sens} = 0.15\%/mV$ ,  $T_{driftrate} = 1^{\circ}C/sec$  and  $V_{driftrate} = 15mV/sec$ , then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

30. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point  $[(175mV - 150mV)/1V/ns]$ .
31. Pulse width of an input signal is defined as the width between the first crossing of  $V_{REF}(DC)$  and the consecutive crossing of  $V_{REF}(DC)$ .
32.  $t_{DQSL}$  describes the instantaneous differential input low pulse width on  $DQS - /DQS$ , as measured from one falling edge to the next consecutive rising edge.
33.  $t_{DQSH}$  describes the instantaneous differential input high pulse width on  $DQS - /DQS$ , as measured from one rising edge to the next consecutive falling edge.
34.  $t_{DQSH,act} + t_{DQSL,act} = 1t_{CK,act}$ ; with  $t_{XYZ,act}$  being the actual measured value of the respective timing parameter in the application.
35.  $t_{DSH,act} + t_{DSS,act} = 1t_{CK,act}$ ; with  $t_{XYZ,act}$  being the actual measured value of the respective timing parameter in the application.
36. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{ERR}(mper),act$  of the input clock, where  $2 \leq m \leq 12$ . (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{ERR}(mper),act,min} = -172ps$  and  $t_{ERR}(mper),act,max} = +193ps$ , then  $t_{DQSK,min}(derated) = t_{DQSK,min} - t_{ERR}(mper),act,max} = -400ps - 193ps = -593ps$  and  $t_{DQSK,max}(derated) = t_{DQSK,max} - t_{ERR}(mper),act,min} = 400ps + 172ps = +572ps$ . Similarly,  $t_{LZ}(DQ)$  for DDR3-800 derates to  $t_{LZ}(DQ),min(derated) = -800ps - 193ps = -993ps$  and  $t_{LZ}(DQ),max(derated) = 400ps + 172ps = +572ps$ . Note that  $t_{ERR}(mper),act,min}$  is the minimum measured value of  $t_{ERR}(nper)$  where  $2 \leq n \leq 12$ , and  $t_{ERR}(mper),act,max}$  is the maximum measured value of  $t_{ERR}(nper)$  where  $2 \leq n \leq 12$ .
37. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT}(per),act$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{CK}(avg),act} = 2500ps$ ,  $t_{JIT}(per),act,min} = -72ps$  and  $t_{JIT}(per),act,max} = +93ps$ , then  $t_{RPRE,min}(derated) = t_{RPRE,min} + t_{JIT}(per),act,min} = 0.9 \times t_{CK}(avg),act} + t_{JIT}(per),act,min} = 0.9 \times 2500ps - 72ps = +2178ps$ . Similarly,  $t_{QH,min}(derated) = t_{QH,min} + t_{JIT}(per),act,min} = 0.38 \times t_{CK}(avg),act} + t_{JIT}(per),act,min} = 0.38 \times 2500ps - 72ps = +878ps$ .

38. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
39. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
40. tCK (avg) is calculated as the average clock period across any consecutive 200cycle window, where each clock period is calculated from rising edge to rising edge.

$$\left( \sum_{j=1}^N tCK_j \right) / N$$

N = 200

41. tCK (abs) is the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK (abs) is not subject to production test.
42. tCH (avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulse.

$$\left( \sum_{j=1}^N tCH_j \right) / (N * tCK_{(avg)})$$

N = 200

43. tCL (avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$\left( \sum_{j=1}^N tCL_j \right) / (N * tCK_{(avg)})$$

N = 200

44. tJIT (duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH (avg). tCL jitter is the largest deviation of any single tCL from tCL (avg). tJIT (duty) is not subject to production test.

tJIT (duty) = Min./Max. of {tJIT (CH), tJIT (CL)}, where:

tJIT (CH) = {tCH<sub>j</sub> - tCH (avg) where j = 1 to 200}

tJIT (CL) = {tCL<sub>j</sub> - tCL (avg) where j = 1 to 200}

45. tJIT (per) is defined as the largest deviation of any single tCK from tCK (avg).

tJIT (per) = Min./Max. of { tCK<sub>j</sub> - tCK (avg) where j = 1 to 200}

tJIT (per) defines the single period jitter when the DLL is already locked. tJIT (per, lck) uses the same definition for single period jitter, during the DLL locking period only. tJIT (per) and tJIT (per, lck) are not subject to production test.

46. tJIT (cc) is defined as the absolute difference in clock period between two consecutive clock cycles:

tJIT (cc) = Max. of {tCK<sub>j+1</sub> - tCK<sub>j</sub>}

tJIT (cc) defines the cycle when the DLL is already locked. tJIT (cc, lck) uses the same definition for cycle-to-cycle jitter, during the DLL locking period only. tJIT (cc) and tJIT (cc, lck) are not subject to production test.

47. tERR (nper) is defined as the cumulative error across n multiple consecutive cycles from tCK (avg).

tERR (nper) is not subject to production test.

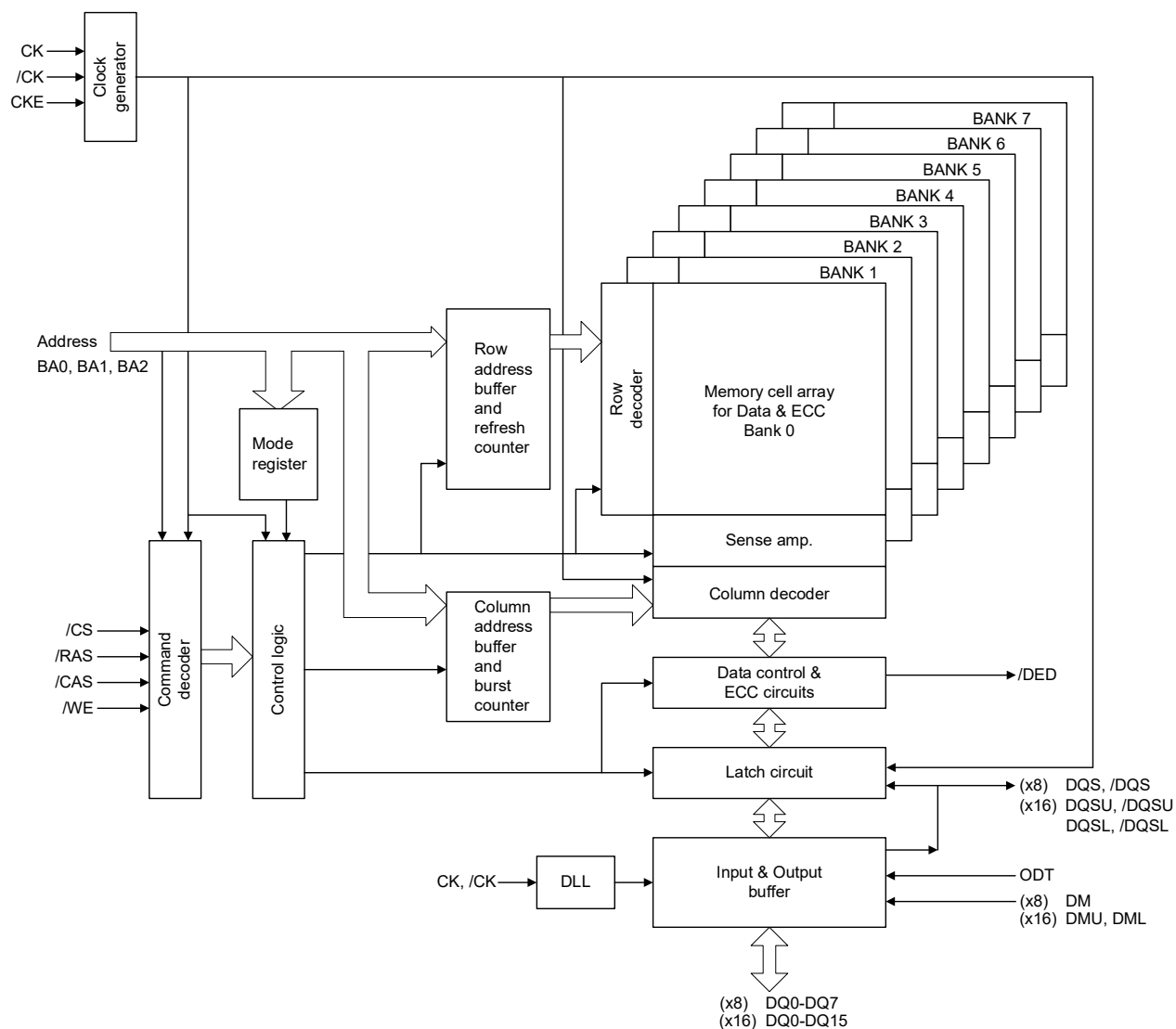
48. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

49. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing hold at all times. (minimum and maximum of spec values are to be used for calculations in the table below.)

Parameter	Symbol	Min.	Max.	Unit
Absolute clock period	tCK (abs)	tCK (avg)min. + tJIT (per)min.	tCK (avg)max. + tJIT (per)max.	ps
Absolute clock high pulse width	tCH (abs)	tCH (avg)min. x tCK (avg)min. + tJIT (duty)min.	tCH (avg)max. x tCK (avg)max. + tJIT (duty)max.	ps
Absolute clock low pulse width	tCL (abs)	tCL (avg)min. x tCK (avg)min. + tJIT (duty)min.	tCL (avg)max. x tCK (avg)max. + tJIT (duty)max.	ps

50. tCH (abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
51. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

## 6. Block Diagram



## 7. Pin Function

### CK, /CK (input pins)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

### /CS (input pin)

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

### /RAS, /CAS, /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

### A0 to A15 (input pins)

Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

#### [Address Pins Table]

Configuration	Page Size	Address (A0 to A15)	
		Row address	Column address
x8	1KB	AX0 to AX15	AY0 to AY9
x16	2KB	AX0 to AX14	AY0 to AY9

### A10(AP) (input pin)

A10 is sampled during read/write commands to determine whether auto precharge should be performed to the accessed bank after the read/write operation. (high: auto precharge; low: no auto precharge) A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

### A12(/BC) (input pin)

A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.

(A12 = high: no burst chop, A12 = low: burst chopped.) See command truth table for details.

### BA0 to BA2 (input pins)

BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine which mode register (MR0 to MR3) is to be accessed during a MRS cycle.

Bank	BA2	BA1	BA0
Bank0	L	L	L
Bank1	L	L	H
Bank2	L	H	L
Bank3	L	H	H
Bank4	H	L	L
Bank5	H	L	H
Bank6	H	H	L
Bank7	H	H	H

Remark: H: VIH, L: VIL

**CKE (input pin)**

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

**DM, DMU, DML (input pins)**

DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS.

**DQ0 to DQ15 (input/output pins)**

Bi-directional data bus.

**DQS, /DQS, DQSU, /DQSU, DQSL, /DQSL (input/output pins)**

Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. The data strobe DQS is paired with differential signal /DQS to provide differential pair signaling to the system during READs and WRITEs.

**/DED (output pin)**

/DED, Double bit Error Detect pin sends a fault detection signal to notify SoC of memory data error state when uncorrectable error is found in DRAM; Compatible with conventional JEDEC standard DRAM; /DED pin is connected or unconnected does not affect ECC function; /DED pin state or level does not affect ECC function; The /DED pin is an open-drain output. /DED pin should be terminated at the VTTD and will be output low level when DED occurs. If you do not use memory error notification through /DED pin, please fix /DED pin to VSS or please keep it as Floating. To reset the output of DED, perform the initialization operation or EXIT of MPR.

**/RESET (input pin)**

/RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD (1.20V for DC high and 0.30V for DC low). It is negative active signal (active low) and is referred to GND. There is no termination required on this signal. It will be heavily loaded across multiple chips. /RESET is destructive to data contents.

**ODT (input pin)**

ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQSU, /DQSU, DQSL, /DQSL, DMU, and DML signal. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

**ZQ (supply)**

Reference pin for ZQ calibration.

**VDD, VSS, VDDQ, VSSQ (power supply pins)**

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

**VREFCA, VREFDQ (power supply pins)**

Reference voltage

## 8. Command Operation

### 8.1. Command Truth Table

The DDR3 SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0-2	A12(/BS)	A10(AP)	A0-A15	Note
		Previous	Current									
Mode register set	MRS	H	H	L	L	L	L	BA	op-code			
Auto refresh	REF	H	H	L	L	L	H	V	V	V	V	
Self refresh entry	SELF	H	L	L	L	L	H	V	V	V	V	6, 8, 11
Self refresh exit	SELEX	L	H	H	X	X	X	X	X	X	X	6, 8, 7
		L	H	L	H	H	H	V	V	V	V	11
Single bank precharge	PRE	H	H	L	L	H	L	BA	V	L	V	
Precharge all banks	PALL	H	H	L	L	H	L	V	V	H	V	
Bank activate	ACT	H	H	L	L	H	H	BA	RA			12
Write(Fixed BL)	WRIT	H	H	L	H	L	L	BA	V	L	CA	
Write(BC4, on the fly)	WRS4	H	H	L	H	L	L	BA	L	L	CA	
Write(BL8, on the fly)	WRS8	H	H	L	H	L	L	BA	H	L	CA	
Write with auto precharge (Fixed BL)	WRITA	H	H	L	H	L	L	BA	V	H	CA	
Write with auto precharge (BC4, on the fly)	WRAS4	H	H	L	H	L	L	BA	L	H	CA	
Write with auto precharge (BL8, on the fly)	WRAS8	H	H	L	H	L	L	BA	H	H	CA	
Read(Fixed BL)	READ	H	H	L	H	L	H	BA	V	L	CA	
Read (BC4, on the fly)	RDS4	H	H	L	H	L	H	BA	L	L	CA	
Read (BL8, on the fly)	RDS8	H	H	L	H	L	H	BA	H	L	CA	
Read with auto precharge (Fixed BL)	READA	H	H	L	H	L	H	BA	V	H	CA	
Read with auto precharge (BC4, on the fly)	RDAS4	H	H	L	H	L	H	BA	L	H	CA	
Read with auto precharge (BL8, on the fly)	RDAS8	H	H	L	H	L	H	BA	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	9
Device deselect	DESL	H	H	H	X	X	X	X	X	X	X	10
Power down mode entry	PDEN	H	L	H	X	X	X	X	X	X	X	5, 11
		H	L	L	H	H	H	V	V	V	V	
Power down mode exit	PDEX	L	H	H	X	X	X	X	X	X	X	5, 11
		L	H	L	H	H	H	V	V	V	V	
ZQ calibration long	ZQCL	H	H	L	H	H	L	X	X	H	X	
ZQ calibration short	ZQCS	H	H	L	H	H	L	X	X	L	X	

Remark:

1. H = VIH; L = VIL; V = VIH or VIL (defined logical level).
2. X = Don't care (defined or undefined, including floating around VREF) logical level.
3. BA = Bank Address. RA = Row Address. CA = Column Address. /BC = Bust Chop.

Notes:

1. All DDR3 commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The most significant bit (MSB) of BA, RA, and CA are device density and configuration dependent.
2. /RESET is an active low asynchronous signal that must be driven high during normal operation
3. Bank Addresses (BA) determines which bank is to be operated upon. For MRS, BA selects a mode register.
4. Burst READs or WRITEs cannot be terminated or interrupted and fixed/on the flyBL will be defined by MRS.
5. The power-down mode does not perform any refresh operations.
6. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
7. Self-refresh exit is asynchronous.
8. VREF (both VREFDQ and VREFCA) must be maintained during self-refresh operation. VREFDQ supply may be turned off and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.
9. The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
10. The DESL command performs the same function as a NOP command.
11. Refer to the CKE Truth Table for more detail with CKE transition.
12. No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

### 8.2. No Operation Command [NOP]

The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

The no operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (/CS low, /RAS, /CAS, /WE high). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

### 8.3. Device Deselect Command [DESL]

The deselect function (/CS high) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

### 8.4. Mode Register Set Command [MR0 to MR3]

The mode registers are loaded via row address inputs. See mode register descriptions in the Programming the mode register section. The mode register set command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

### 8.5. Bank Activate Command [ACT]

This command is used to open (or activate) a row in a particular bank for a subsequent access. The values on the BA inputs select the bank, and the address provided on row address inputs selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

4. Notes:
5. No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.



#### **8.6. Read Command [READ, RDS4, RDS8, READA, RDAS4, RDAS8]**

The read command is used to initiate a burst read access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

#### **8.7. Write Command [WRIT, WRS4, WRS8, WRITA, WRAS4, WRAS8]**

The write command is used to initiate a burst write access to an active row. The values on the BA inputs select the bank, and the address provided on column address inputs selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to memory; if the DM signal is registered high, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

#### **8.8. Precharge Command [PRE, PALL]**

The precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA select the bank. Otherwise, BA are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any read or write commands being issued to that bank. A precharge command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

#### **8.9. Auto precharge Command [READA, WRITA]**

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the DDR3 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge, a read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is (AL\* + tRTP) cycles later from the read with auto precharge command.

Auto precharge can also be implemented during write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS latency) thus improving system performance for random data access. The tRAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Note: AL (Additive Latency), refer to Posted /CAS description in the Register Definition section.

#### **8.10. Auto-Refresh Command [REF]**

Auto-refresh is used during normal operation of the DDR3 SDRAM and is analogous to /CAS-before-/RAS (CBR) refresh in FPM/EDO DRAM. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an auto-refresh command.

A maximum of eight auto-refresh commands can be posted to any given DDR3, meaning that the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 9 x tREFI. This maximum absolute interval is to allow DDR3 output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

#### **8.11. Self-Refresh Command [SELF]**

The self-refresh command can be used to retain data in the DDR3, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 retains data without external clocking. The self-refresh command is initiated like an auto-refresh command except CKE is disabled (low). The DLL is automatically disabled upon entering self-refresh and is automatically enabled and reset upon exiting self-refresh. The active termination is also disabled upon entering self-refresh and enabled upon exiting self-refresh. (512 clock cycles must then occur before a read command can be issued). Input signals except CKE are "Don't Care" during self-refresh. The procedure for exiting self-refresh requires a sequence of commands. First, CK and /CK must be stable prior to CKE going back high. Once CKE is high, the DDR3 must have NOP commands issued for tXSDLL because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 512 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

#### **8.12. ZQ calibration Command [ZQCL, ZQCS]**

ZQ calibration command (short or long) is used to calibrate DRAM RON and ODT values over PVT. ZQ Calibration Long (ZQCL) command is used to perform the initial calibration during power-up initialization sequence.

ZQ Calibration Short (ZQCS) command is used to perform periodic calibrations to account for VT variations. All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh.

### 8.13. CKE Truth Table

[CKE Truth Table]

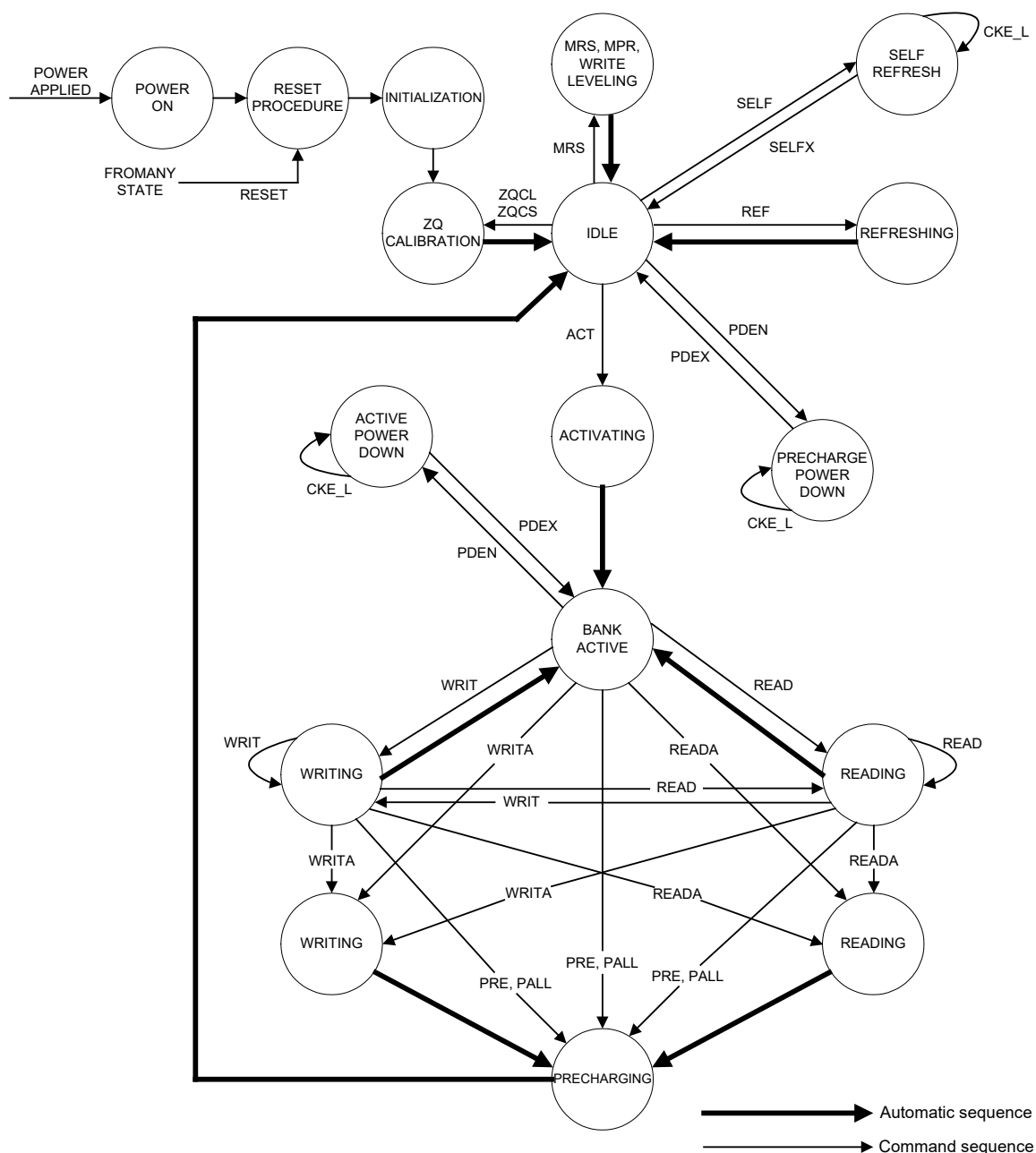
Current state* <sup>2</sup>	CKE		Command (n) <sup>*3</sup> /CS, /RAS, /CAS, /WE	Operation (n) <sup>*3</sup>	Notes
	Previous cycle (n-1) <sup>*1</sup>	Current cycle (n) <sup>*1</sup>			
Power-down			×	Maintain power-down	14, 15
	L	H	DESL or NOP	Power-down exit	11, 14
Self-refresh	L	L	×	Maintain self-refresh	15, 16
	L	H	DESL or NOP	Self-refresh exit	8, 12, 16
Bank Active	H	L	DESL or NOP	Active power-down entry	11, 13, 14
Reading	H	L	DESL or NOP	Power-down entry	11, 13, 14, 17
Writing	H	L	DESL or NOP	Power-down entry	11, 13, 14, 17
Precharging	H	L	DESL or NOP	Power-down entry	11, 13, 14, 17
Refreshing	H	L	DESL or NOP	Precharge power-down entry	11
All banks idle	H	L	DESL or NOP	Precharge power-down entry	11, 13, 14, 18
	H	L	REFRESH	Self-refresh entry	9, 13, 18
Any state other than listed above	H	H	Refer to the Command Truth Table		10

Remark: H = VIH. L = VIL. × = Don't care

Notes:

1. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) is the state of CKE at the previous clock edge.
2. Current state is the state of the DDR3 SDRAM immediately prior to clock edge n.
3. Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n). ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self-refresh.
6. CKE must be registered with the same value on tCKE (min.) consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKE (min.) clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKE (min.) + tIH.
7. DESL and NOP are defined in the Command Truth Table.
8. On self-refresh exit, DESL or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT command may be issued only after tXSDLL is satisfied.
9. Self-refresh mode can only be entered from the all-banks idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for power-down entry and exit are NOP and DESL only.
12. Valid commands for self-refresh exit are NOP and DESL only.
13. Self-refresh can not be entered while read or write operations, (extended) mode register set operations or precharge operations are in progress. See section Power-Down and self-refresh Command for a detailed list of restrictions.
14. The power-down does not perform any refresh operations.
15. "×" means "don't care" (including floating around VREF) in self-refresh and power-down. It also applies to address pins.
16. VREF (both VREFDQ and VREFCA) must be maintained during self-refresh operation. VREFDQ supply may be turned off and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, the precharge power-down is entered, otherwise active power-down is entered.
18. Idle state means that all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress. CKE is high and all timings from previous operation are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all self-refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXPDLL, etc.).

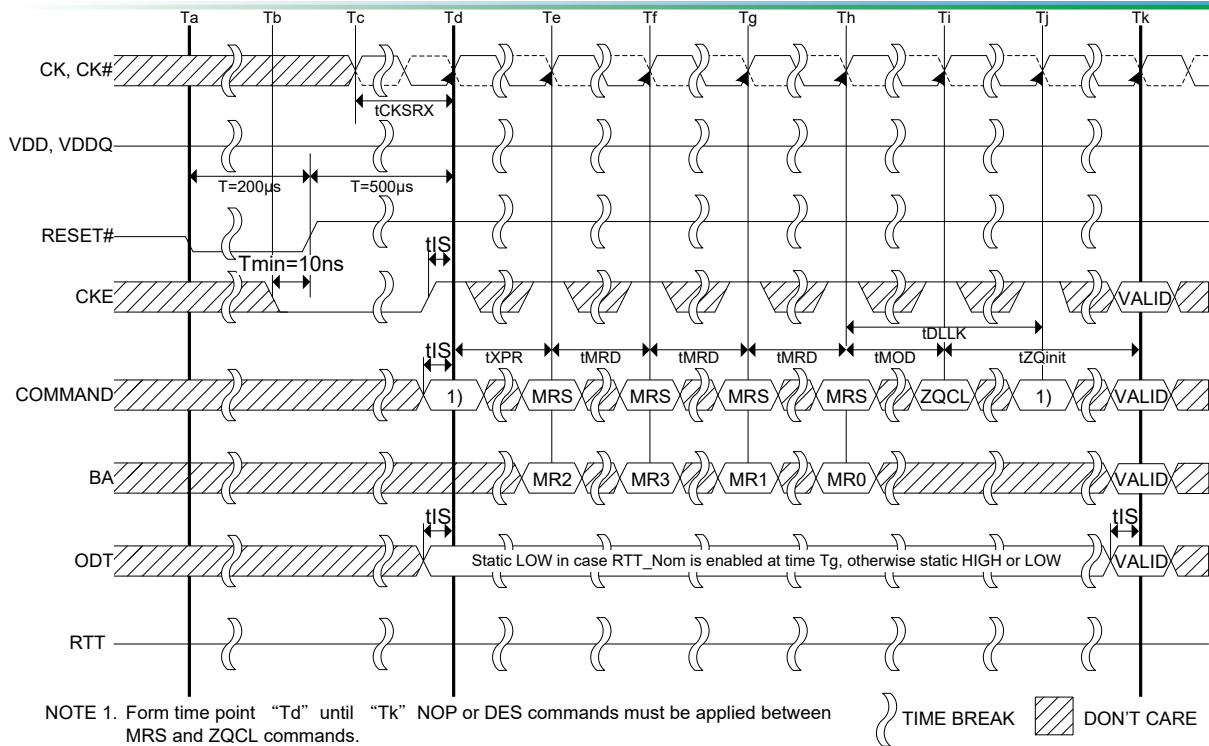
### 9.1. Simplified State Diagram



## 9.2. RESET and Initialization Procedure

### 9.2.1. Power-Up and Initialization Sequence

1. Apply power
  - /RESET is recommended to be maintained below  $0.2 \times VDD$ ; all other inputs may be undefined.
  - /RESET needs to be maintained for minimum 200us with stable power. CKE is pulled low anytime before /RESET being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to VDD (min.) must be no greater than 200ms; and during the ramp,  $VDD > VDDQ$  and  $(VDD - VDDQ) < 0.3V$ .
  - VDD and VDDQ are driven from a single power converter output
- AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95V max once power ramp is finished,
- AND
  - VREF tracks  $VDDQ/2$ .
- OR
  - Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT and VREF.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After /RESET is de-asserted, wait for another 500us until CKE become active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, /CK) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also a NOP or DESL command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "high" after Reset, CKE needs to be continuously registered high until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM will keep its on-die termination in high-impedance state during /RESET being asserted at least until CKE being registered high. Therefore, the ODT signal may be in undefined state until tIS before CKE being registered high. After that, the ODT signal must be kept inactive (low) until the power-up and initialization sequence is finished, including expiration of tDLLK and tZQinit.
5. After CKE being registered high, wait minimum of tXPR, before issuing the first MRS command to load mode register. ( $tXPR = \max. (tXS; 5 \times tCK)$ )
6. Issue MRS command to load MR2 with all application settings. (To issue MRS command for MR2, provide low to BA0 and BA2, high to BA1.)
7. Issue MRS command to load MR3 with all application settings. (To issue MRS command for MR3, provide low to BA2, high to BA0 and BA1.)
8. Issue MRS command to load MR1 with all application settings and DLL enabled. (To issue DLL Enable command, provide low to A0, high to BA0 and low to BA1 and BA2).
9. Issue MRS command to load MR0 with all application settings and DLL reset. (To issue DLL reset command, provide high to A8 and low to BA0 to BA2).
10. Issue ZQCL command to start ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

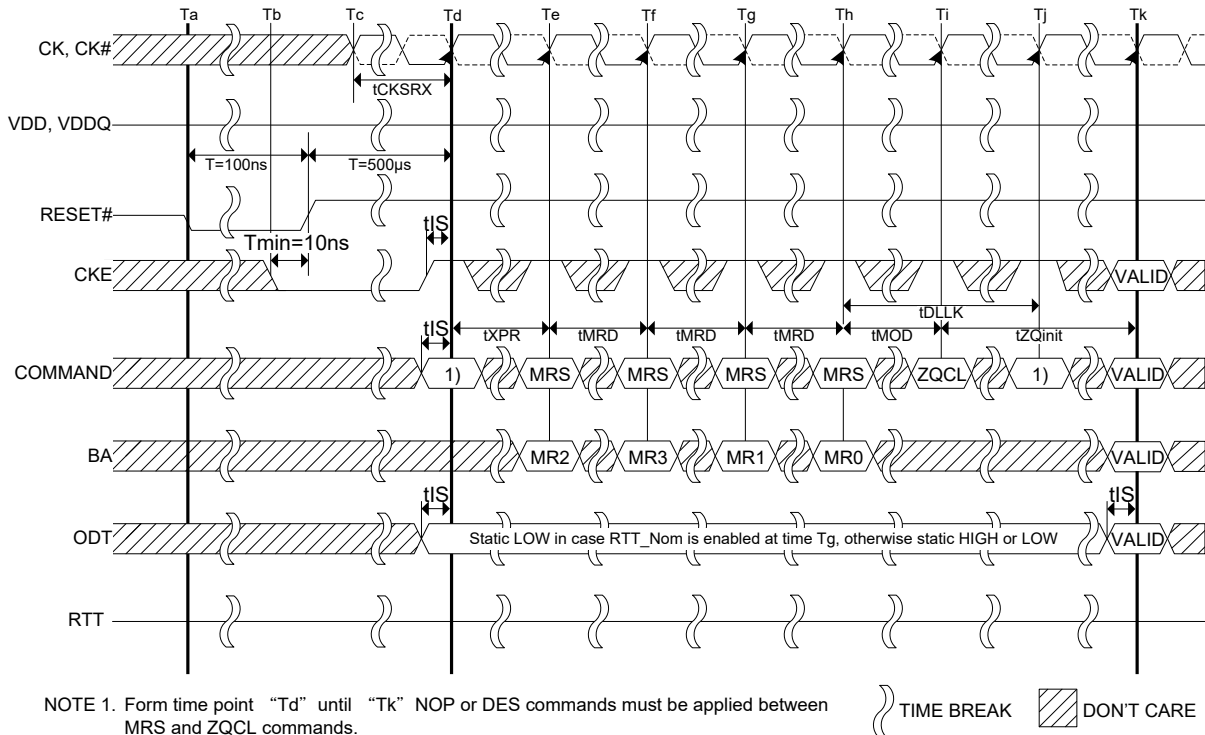


#### Reset and Initialization Sequence at Power-On Ramping

##### 9.2.2. Reset Initialization with Stable Power

The following sequence is required for /RESET at no power interruption initialization.

1. Assert /RESET below  $0.2 \times VDD$  anytime when reset is needed (all other inputs may be undefined). /RESET needs to be maintained for minimum 100ns. CKE is pulled low before /RESET being de-asserted (minimum time 10ns).
2. Follow Power-Up Initialization Sequence steps 2 to 11.
3. The reset sequence is now completed; DDR3 SDRAM is ready for normal operation.



#### Reset Procedure at Power Stable Condition

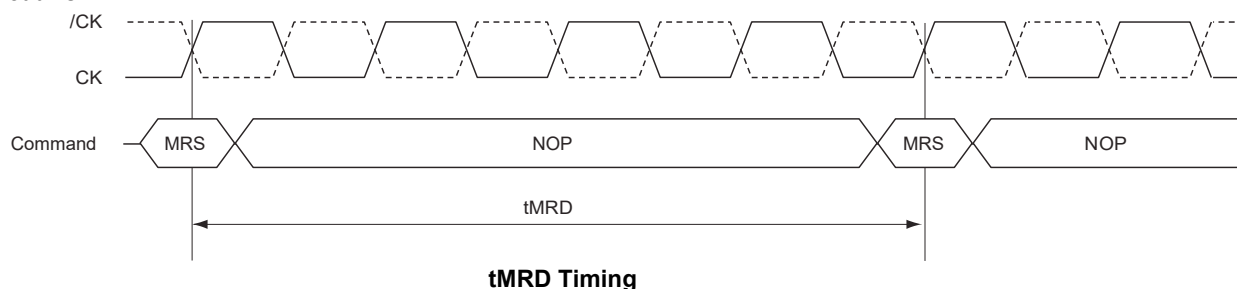
### 9.3. Programming the Mode Register

For application flexibility, various functions, features and modes are programmable in four mode registers, provided by the DDR3 SDRAM, as user defined variables, and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, content of mode registers must be fully initialized and/or re-initialized, i.e. written, after Power-up and/or reset for proper operation. Also the contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset does not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands. The MRS command to non-MRS command delay, tMOD, is required for the DRAM to update the features except DLL reset and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is already high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

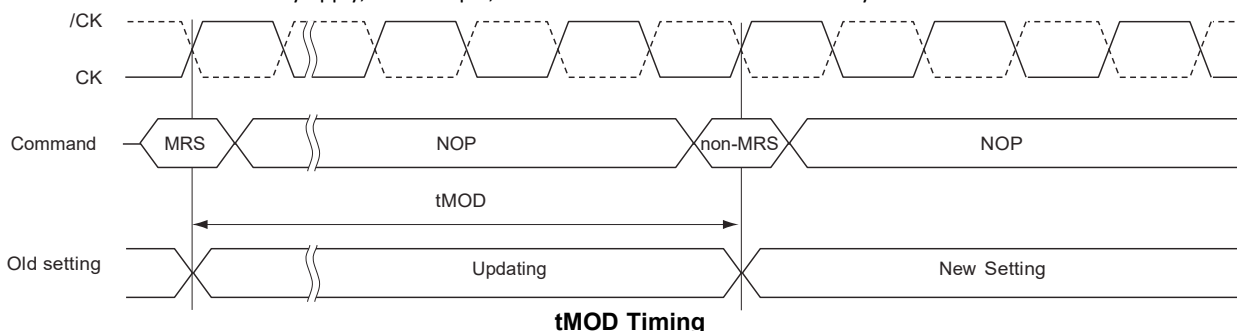
#### Mode Register Set Command Cycle Time (tMRD)

tMRD is the minimum time required from an MRS command to the next MRS command. As DLL enable and DLL reset are both MRS commands, tMRD is applicable between MRS to MR1 for DLL enable and MRS to MR0 for DLL reset, and not tMOD.



#### MRS Command to Non-MRS Command Delay (tMOD)

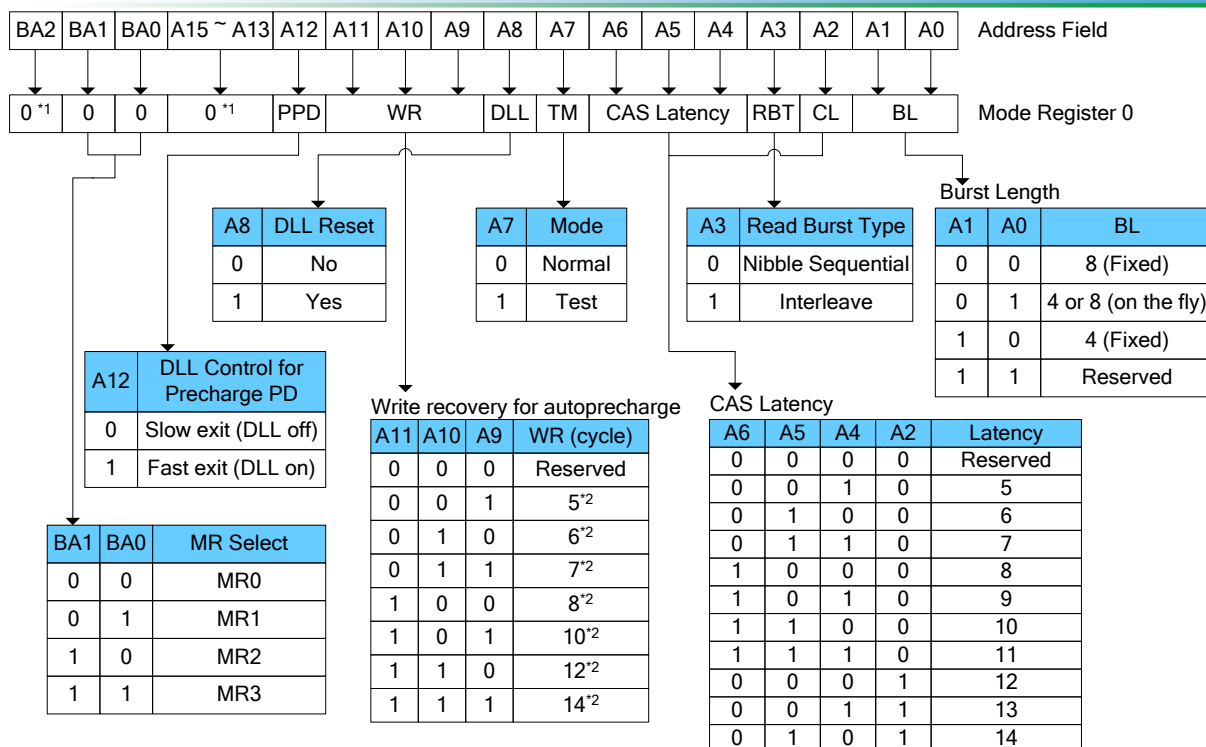
tMOD is the minimum time required from an MRS command to a non-MRS command excluding NOP and DESL. Note that additional restrictions may apply, for example, MRS to MR0 for DLL reset followed by read.



### 9.4. DDR3 SDRAM Mode Register 0 [MR0]

The Mode Register MR0 stores the data for controlling various operating modes of DDR3 SDRAM.

It controls burst length, read burst type, /CAS latency, test mode, DLL reset, WR and DLL control for precharge power-down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0, BA1 and BA2, while controlling the states of address pins according to the table below.



#### Notes:

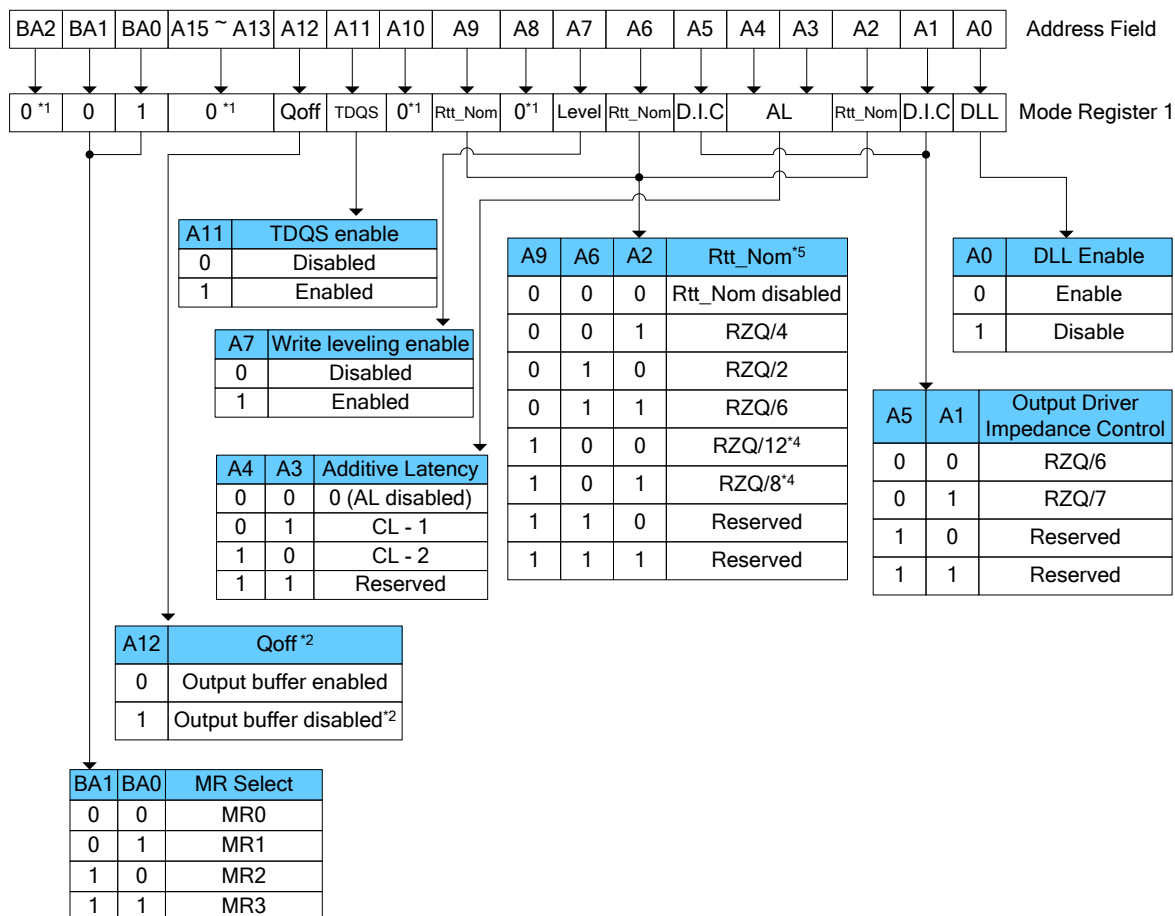
- BA2 and A13 ~ A15 are reserved for future use and must be programmed to 0 during MRS.
- WR (Write Recovery for auto-precharge) min in clock cycle is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer:
  - WR min [cycles] = roundup (tWR [ns] / tCK [ns]).
  - The WR value in the mode register must be programmed to be equal or larger than WR min. The programmed WR value is used with tRP to determine tDAL.

#### MRO Programming



### 9.5. DDR3 SDRAM Mode Register 1 [MR1]

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, RTT\_Nom impedance, additive latency, write leveling enable and Qoff. The Mode Register 1 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA0 and low on BA1, while controlling the states of address pins according to the table below.



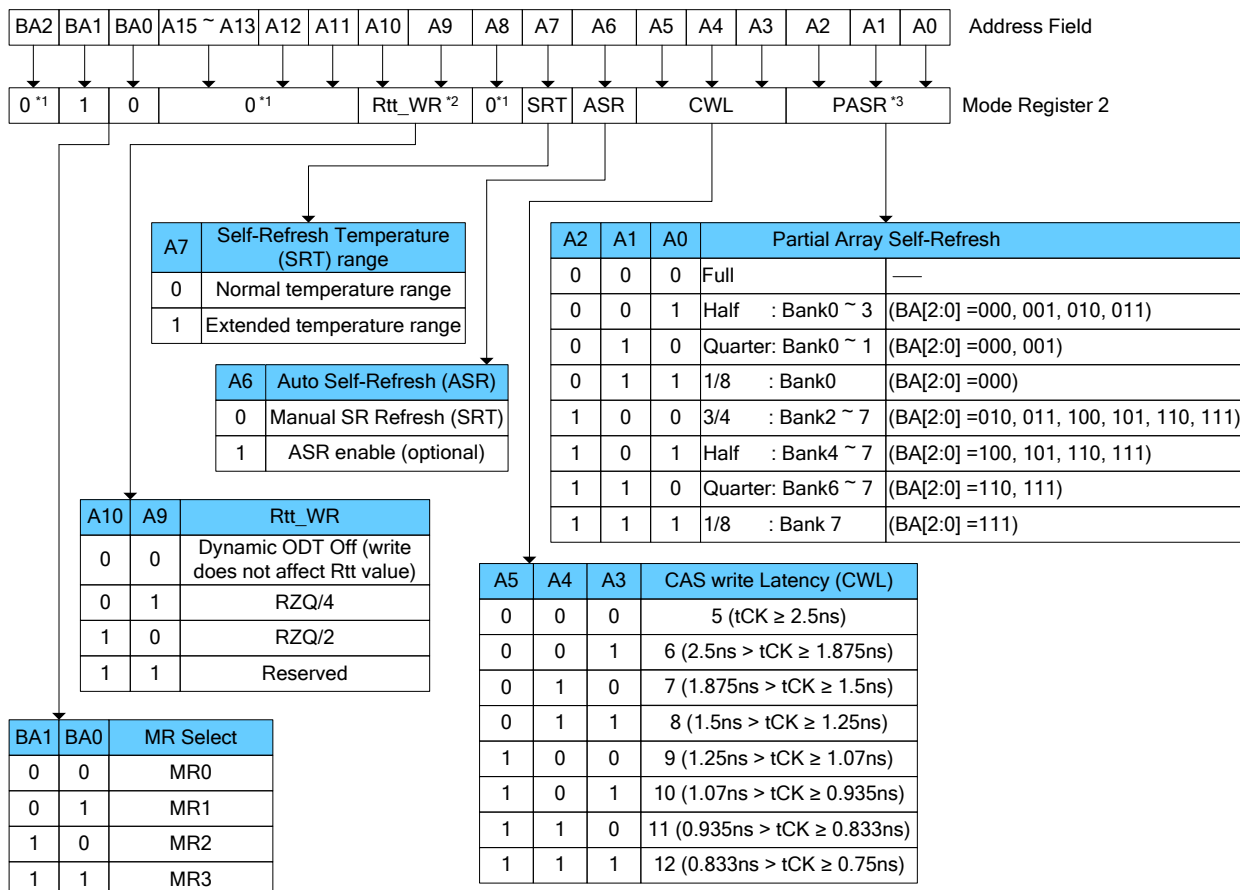
#### Notes:

1. BA2, A8, A10, A11 and A13 ~ A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.
2. Outputs disabled - DQ, DQS, /DQS.
3. RZQ = 240 Ohm
4. If RTT\_Nom is used during writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.
5. In write leveling mode (MR1[bit7] = 1) with MR1[bit12] = 1, all RTT\_Nom settings are allowed; in write leveling mode (MR1[bit7] = 1) with MR1[bit12] = 0, only RTT\_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed

#### MR1 Programming

### 9.6. DDR3 SDRAM Mode Register 2 [MR2]

The Mode Register MR2 stores the data for controlling refresh related features, Rtt\_WR impedance and /CAS write latency (CWL). The Mode Register 2 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and low on BA0, while controlling the states of address pins according to the table below.



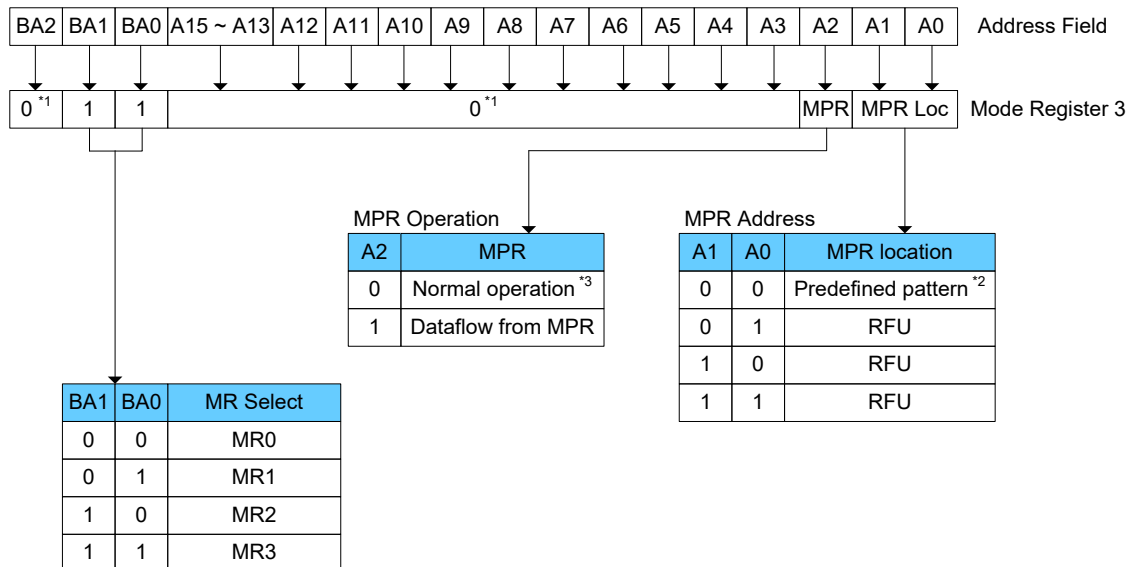
Notes:

1. BA2, A8 and A11 to A15 are RFU and must be programmed to 0 during MRS.
2. The Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled. During write leveling, Dynamic ODT is not available.
3. Optional in DDR3 SDRAM: If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self-refresh is entered. Data integrity will be maintained if tREF conditions are met and no self-refresh command is issued.

#### MR2 Programming

### 9.7. DDR3 SDRAM Mode Register 3 [MR3]

The Mode Register MR3 controls Multi Purpose Registers (MPR). The Mode Register 3 is written by asserting low on /CS, /RAS, /CAS, /WE, high on BA1 and BA0, while controlling the states of address pins according to the table below.



4.

Notes :

1. BA2, A3 to A15 are reserved for future use (RFU) and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation, MR3 A[2]=0, MR3 A[1:0] will be ignored.

#### MR3 Programming

## 9.8. Extended Temperature Usage(MR2)

### [Mode Register Description]

Field	Bits	Description
ASR	MR2 (A6)	<b>Auto Self-Refresh (ASR)</b> when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TC during subsequent Self-Refresh operation 0 = Manual SR Reference (SRT) 1 = ASR enable
SRT	MR2 (A7)	<b>Self-Refresh Temperature (SRT) Range</b> If ASR = 0, the SRT bit must be programmed to indicate TC during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended (optional) operating temperature range

### Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in figure of MR2 programming will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

### Auto Self-Refresh Mode - ASR Mode

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1 and MR2 bit A7 = 0. The DRAM will manage self-refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage self-refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0.

If the ASR mode is not enabled (MR2 bit A6 = 0), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during self-refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range.

### Self-Refresh Temperature Range - SRT

If ASR = 0, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = 0, then the DRAM will set an appropriate refresh rate for self-refresh operation in the Normal Temperature Range. If SRT = 1 then the DRAM will set an appropriate, potentially different, refresh rate to allow self-refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0 and the DRAM should not be operated outside the Normal Temperature Range.

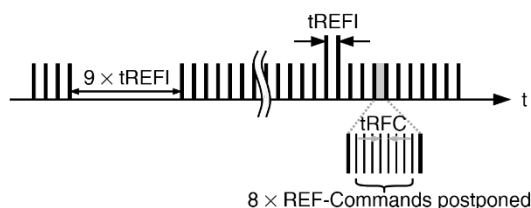
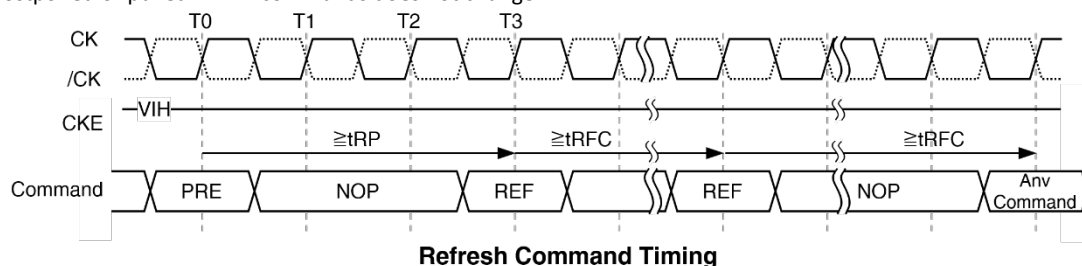
### [Self-Refresh Mode Summary]

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 - 85°C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 - 95°C)
1	0	ASR enabled. Self-Refresh power consumption is temperature dependent	Normal (0 - 85°C)
1	0	ASR enabled. Self-Refresh power consumption is temperature dependent	Normal and Extended (0 - 95°C)
1	1	Illegal	

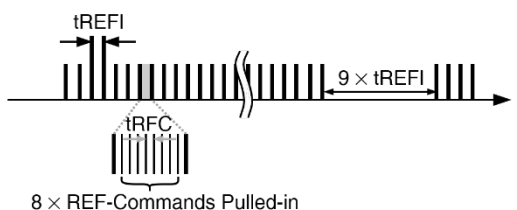
### 9.9. Refresh Command

The refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non-persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires refresh cycles at an average periodic interval of tREFI. When /CS, /RAS and /CAS are held low and /WE high at the rising edge of the clock, the chip enters a refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the refresh command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the refresh command and the next valid command, except NOP or DESL, must be greater than or equal to the minimum refresh cycle time tRFC(min) as shown in the following figure. Note that the tRFC timing parameter depends on memory density.

In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 refresh commands are allowed to be postponed. In case that 8 refresh commands are postponed in a row, the resulting maximum interval between the surrounding refresh commands is limited to  $9 \times \text{tREFI}$ . A maximum of 8 additional refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular refresh commands required later by one. Note that pulling in more than 8 refresh commands in advance does not further reduce the number of regular refresh commands required later, so that the resulting maximum interval between two surrounding refresh commands is limited to  $9 \times \text{tREFI}$ . At any given time, a maximum of 16 REF commands can be issued within  $2 \times \text{tREFI}$ . Self-refresh mode may be entered with a maximum of eight refresh commands being postponed. After exiting self-refresh mode with one or more refresh commands postponed, additional refresh commands may be postponed to the extent that the total number of postponed refresh commands (before and after the self-refresh) will never exceed eight. During self-refresh mode, the number of postponed or pulled-in REF commands does not change.



## Postponing Refresh Command



### Pulling-in Refresh Command

### 9.10. Self-Refresh Operation

The self-refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the self-refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate self-refresh operation. The self-refresh entry (SELF) command is defined by having /CS, /RAS, /CAS and CKE held low with /WE high at the rising edge of the clock.

Before issuing the self-refresh entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) Also, on-die termination must be turned off before issuing self-refresh entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the self-refresh entry command or using MRS to MR1 command. Once the self-refresh entry command is registered, CKE must be held low to keep the device in self-refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is automatically disabled upon entering self-refresh and is automatically enabled (including a DLL-Reset) upon exiting self-refresh.

When the DDR3 SDRAM has entered self-refresh mode all of the external control signals, except CKE and /RESET, are "don't care". For proper self-refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFCA and VREFDQ) must be at valid levels. VREFDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during self-refresh operation, provided that VREFDQ is valid and stable prior to CKE going back high and that first write operation or first write leveling activity may not occur earlier than 512 nCK after exit from self-refresh. The DRAM initiates a minimum of one refresh command internally within tCKESR period once it enters self-refresh mode.

The clock is internally disabled during self-refresh operation to save power. The minimum time that the DDR3 SDRAM must remain in self-refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE cycles after self-refresh entry is registered, however, the clock must be restarted and stable tCKSRX clock cycles before the device can exit self-refresh operation. To protect DRAM internal delay on CKE line to block the input signals, one NOP (or DESL) command is needed after self-refresh entry.

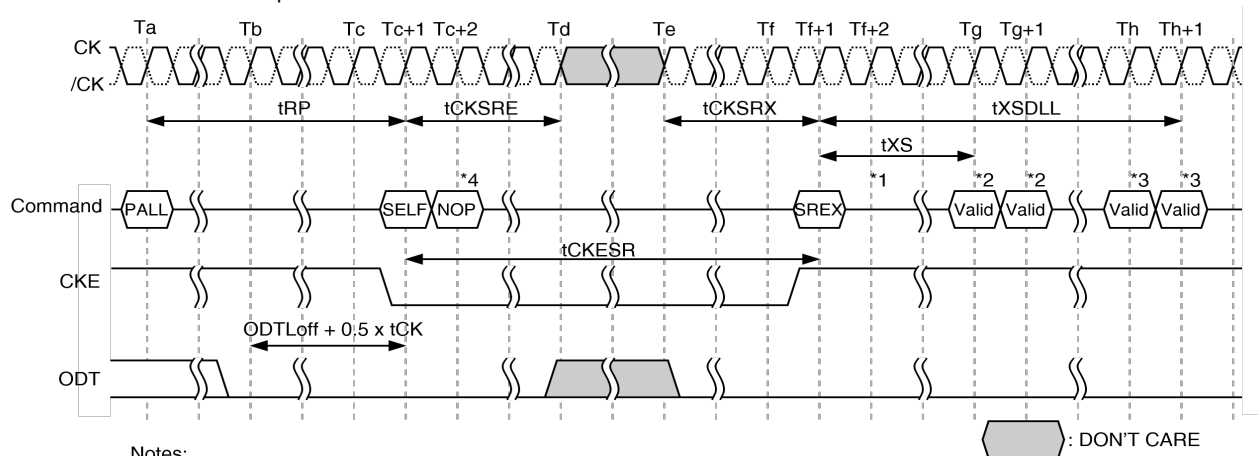
The procedure for exiting self-refresh requires a sequence of events. First, the clock must be stable prior to CKE going back high. Once a self-refresh exit command (SREX, combination of CKE going high and either NOP or DESL on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress.

Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL must be satisfied.

Depending on the system environment and the amount of time spent in self-refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in ZQ Calibration section. To issue ZQ calibration commands, applicable timing requirements must be satisfied (See Figure ZQ Calibration).

CKE must remain high for the entire self-refresh exit period tXSDLL for proper operation except for self-refresh re-entry. Upon exit from self-refresh, the DDR3 SDRAM can be put back into self-refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or DESL commands must be registered on each positive clock edge during the self-refresh exit interval tXS. ODT must be turned off during tXSDLL.

The use of self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into self-refresh mode.



Self-Refresh Entry and Exit Timing

### 9.11. DLL-off Mode

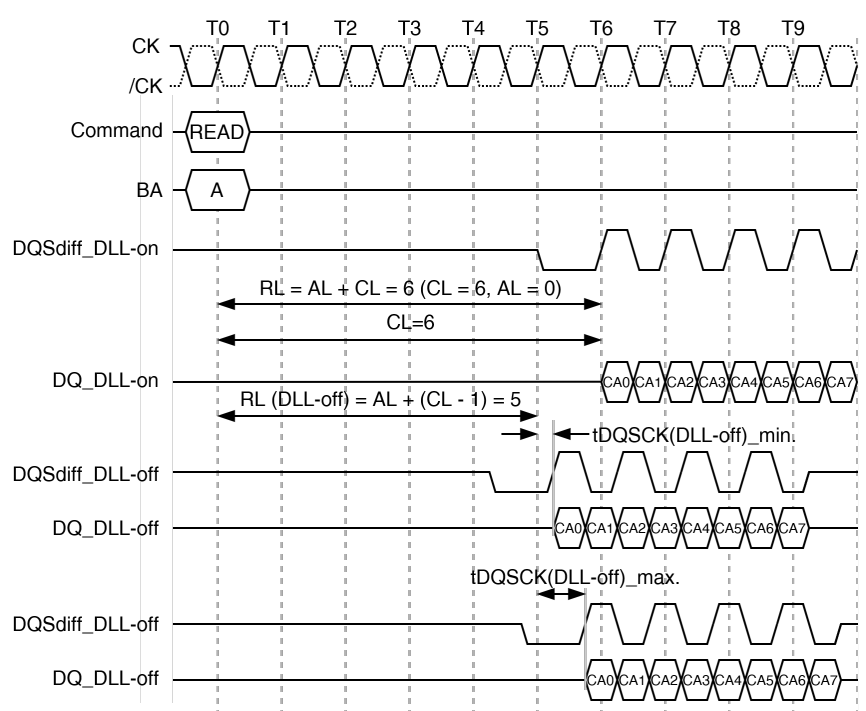
DDR3 DLL-off mode is entered by setting MR1 bit A0 to 1; this will disable the DLL for subsequent operations until A0 bit set back to 0. The MR1 A0 bit for DLL control can be switched either during initialization or later.

The DLL-off mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off mode is specified by the parameter tCKDLL\_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of /CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL = 6 and CWL = 6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK) but not the Data Strobe to Data relationship (tDQSQ, tQH, tQHS). Special attention is needed to line up Read data to controller time domain. Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL + CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL + CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCK (min.) and tDQSCK (max.) is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation are shown at following Timing Diagram (CL = 6, BL8):



**DLL-Off Mode Read Timing Operation**

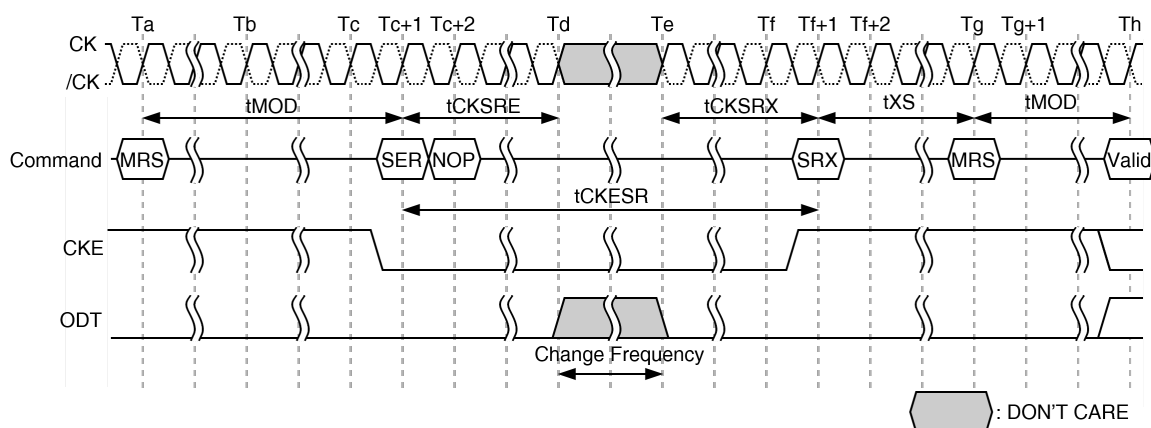
### 9.12. DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to “1”; this will disable the DLL for subsequent operations until A0 bit set back to “0”.

#### DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during self-refresh outlined in the following procedure:

1. Starting from Idle state (all banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 Bit A0 to “1” to disable the DLL.
3. Wait tMOD.
4. Enter self-refresh mode; wait until (tCKSRE) satisfied.
5. Change frequency, in guidance with Input Clock Frequency Change during Precharge Power-Down section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs. After stable clock, wait tCKSRX before issuing SRX command.
7. Starting with the self-refresh exit command, CKE must continuously be registered high until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self-refresh mode was entered, the ODT signal must continuously be registered low until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when self-refresh mode was entered, ODT signal can be registered low or high.
8. Wait tXS, then set mode registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, then DRAM is ready for next command.



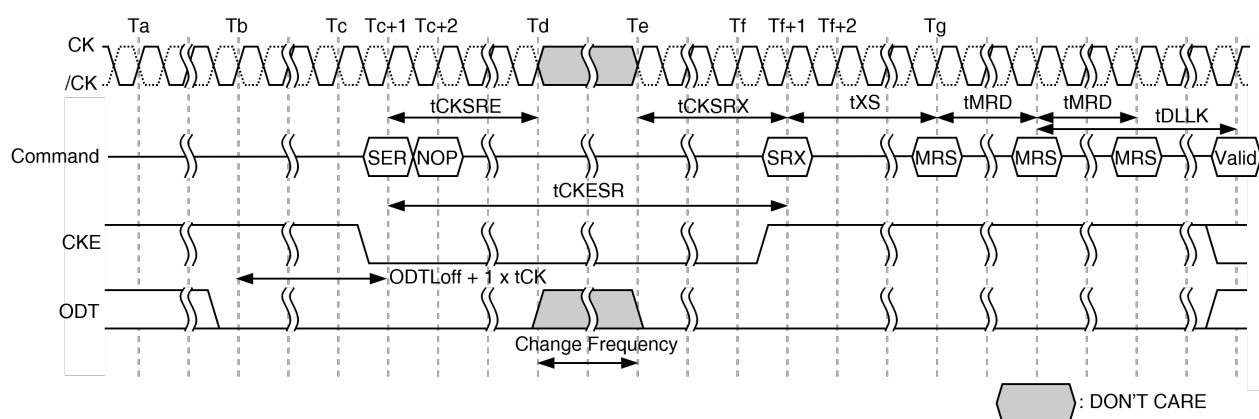
**DLL Switch Sequence from DLL-on to DLL-off**



### DLL "off" to DLL "on" Procedure

To Switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

- Starting from Idle state (all banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
- Enter Self-refresh Mode, wait until tCKSRE satisfied.
- Change frequency, in guidance with Input Clock Frequency Change during Precharge Power-Down section.
- Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
- Starting with the self-refresh exit command, CKE must continuously be registered high until all tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when self-refresh mode was entered, the ODT signal must continuously be registered low until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self-refresh mode was entered, ODT signal can be registered low or high.
- Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
- Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
- Wait tMRD, and then set mode registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
- Wait for tMOD, and then DRAM is ready for next command (remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL). In addition, wait also for tZQoper in case a ZQCL command was issued.



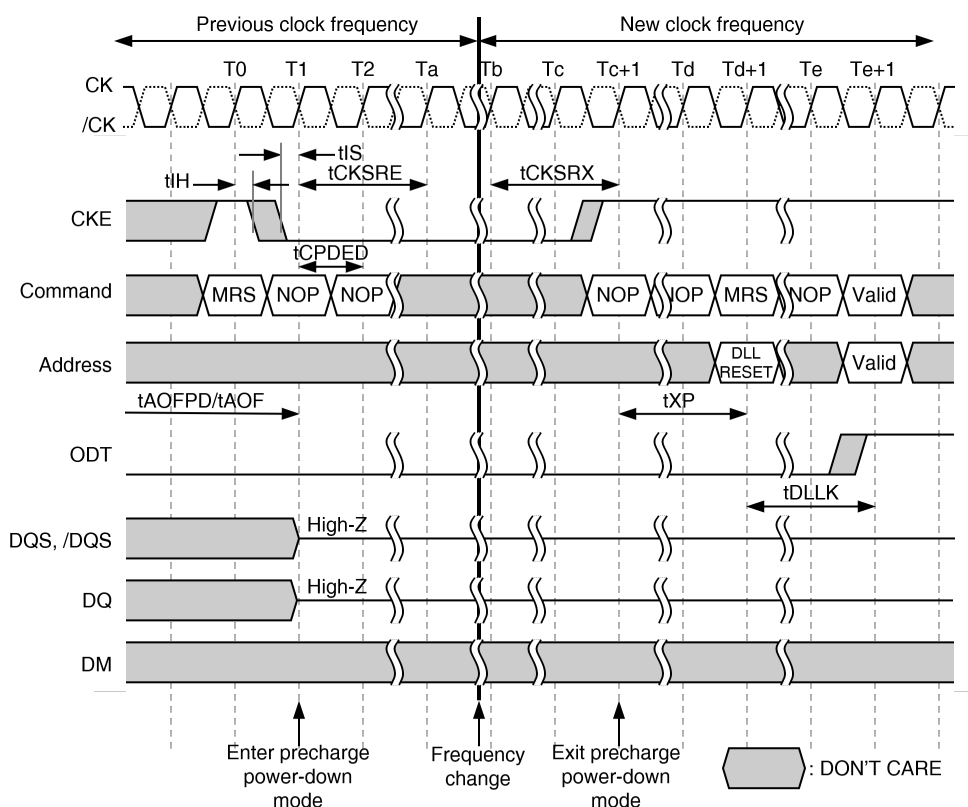
DLL Switch Sequence from DLL-Off to DLL-On

### 9.13. Input clock frequency change

Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (Spread Spectrum Clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) self-refresh mode and (2) precharge power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and  $t_{CKSRE}$  has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to  $t_{CKSRX}$ . When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the self-refresh entry and exit specifications must still be met as outlined in Self-Refresh section.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode.) ODT must be at a logic low ensuring RTT is in an off state prior to entering Precharge Power-down mode and CKE must be at a logic low. A minimum of  $t_{CKSRE}$  must occur after CKE goes low before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable low levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM  $t_{CKSRX}$  before Precharge Power-down may be exited; after Precharge Power-down is exited and  $t_{XP}$  has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high.

During DLL reload period, ODT must remain low. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in the figure Clock Frequency Change in Precharge Power-Down Mode.



#### Notes:

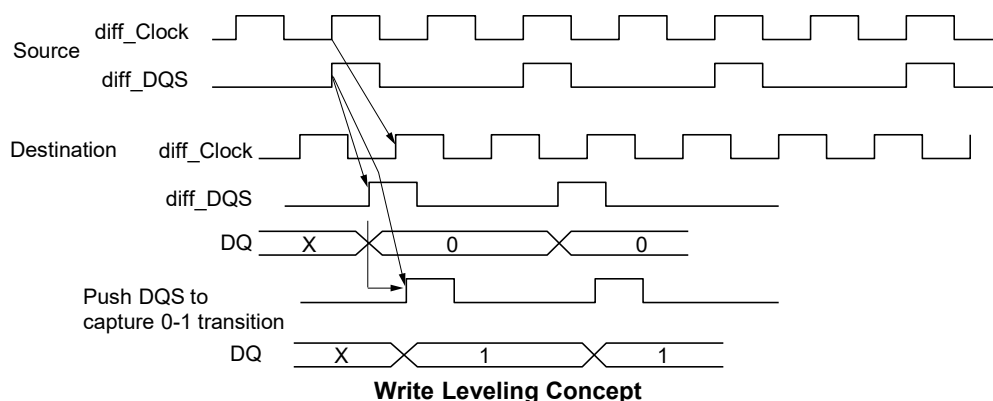
1. Applicable for both slow exit and fast exit precharge power-down.
2.  $t_{CKSRE}$  and  $t_{CKSRX}$  are self-refresh mode specifications but the values they represent are applicable here.
3.  $t_{AOFPD}$  and  $t_{AOF}$  must be satisfied and outputs high-z prior to T1; refer to ODT timing for exact requirements.

### Clock Frequency Change in Precharge Power-Down Mode

### 9.14. Write Leveling(MR1)

For better signal integrity, DDR3 memory module adopts fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits for reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes Controller hard to maintain tDQSS, tDSS and tDSH specification. Therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate the skew.

Write leveling is a scheme to adjust DQS to CK relationship by the controller, with a simple feedback provided by the DRAM. The memory controller involved in the leveling must have adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established through this exercise would ensure tDQSS, tDSS and tDSH specification. A conceptual timing of this scheme is shown as below.



DQS, /DQS driven by the controller during leveling mode must be terminated by the DRAM, based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations  $\times 16$ . On a  $\times 16$  device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff\_DQS (diff\_DQSU) to clock relationship whereas the lower data bits would indicate the lower diff\_DQS (diff\_DQSL) to clock relationship.

#### 9.14.1. DRAM Setting for Write Leveling and DRAM Termination Function in That Mode

DRAM enters into write leveling mode if A7 in MR1 set 1. And after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 0 (MR1 Setting Involved in the Leveling Procedure table).

Note that in write leveling mode, only DQS/DQS terminations are activated and deactivated via ODT pin, not like normal operation (refer to the DRAM Termination Function in The Leveling Mode table)

##### [MR1 Setting Involved in the Leveling Procedure]

Function	MR1 bit	Enable	Disable	Notes
Write leveling enable	A7	1	0	
Output buffer mode (Qoff)	A12	0	1	1

Note: 1. Output buffer mode definition is consistent with DDR2

##### [DRAM Termination Function in The Leveling Mode]

ODT pin@DRAM	DQS, /DQS termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

Note: In write leveling mode with its output buffer disabled (MR1 [bit7] = 1 with MR1 [bit12] = 1) all RTT\_Nom settings are allowed; in write leveling mode with its output buffer enabled (MR1 [bit7] = 1 with MR1 [bit12] = 0) only RTT\_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

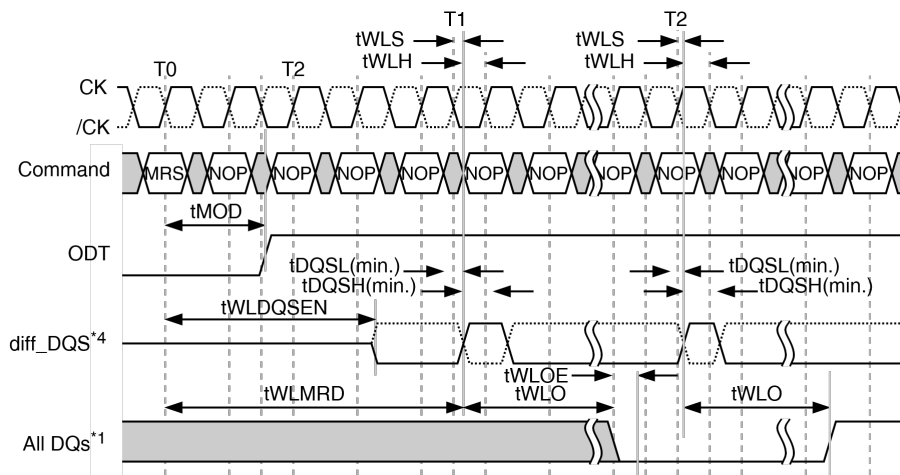
### 9.14.2. Write Leveling Procedure

Memory controller initiates leveling mode of all DRAMs by setting bit 7 of MR1 to 1. Since the controller levelizes rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and /DQS high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tWLMRD, controller provides a single DQS, /DQS edge which is used by the DRAM to sample CK driven from controller. tWLMRD timing is controller dependent.

DRAM samples CK status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS, /DQS) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS delay setting and launches the next DQS, /DQS pulse after some time, which is controller dependent.

Once a 0 to 1 transition is detected, the controller locks DQS delay setting and write leveling is achieved for the device. The below figure describes detailed timing diagram for overall procedure and the timing parameters are shown in below figure.



#### Notes:

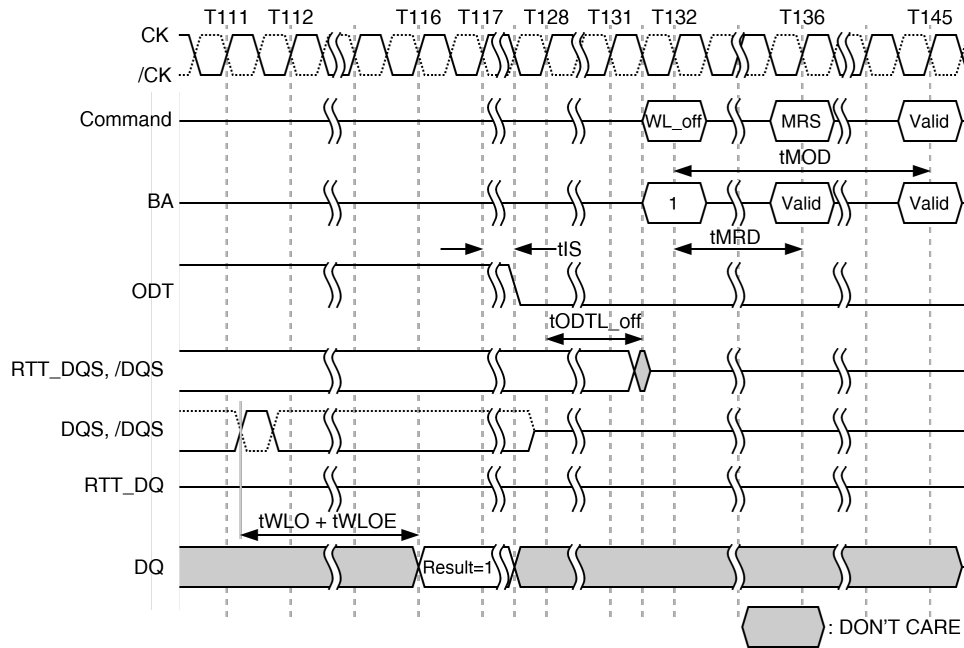
1. DDR3 SDRAM drives leveling feedback on all DQs.
2. MRS : Load MR1 to enter write leveling mode.
3. NOP : NOP or deselection
4. diff\_DQS is the differential data strobe (DQS, /DQS). Timing reference points are the zero crossing. DQS is shown with solid line, /DQS is shown with dotted line.
5. CK, /CK : CK is shown with solid dark line, where as /CK is drawn with dotted line.
6. DQS needs to fulfill minimum pulse width requirements tDQSH (min.) and tDQSL (min.) as defined for regular writes; the max pulse width is system dependent.

### Timing Details Write Leveling Sequence

### 9.14.3. Write Leveling Mode Exit

The following sequence describes how the write leveling mode should be exited:

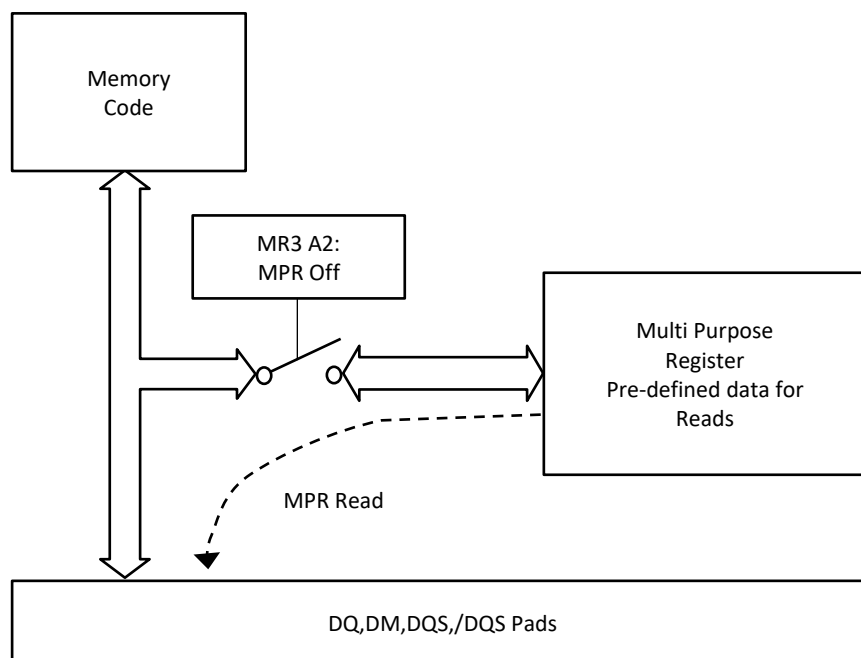
1. After the last rising strobe edge (see T111), stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (T145).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low (see T128).
3. After the RTT is switched off: disable Write Level Mode via MR command (see T132).
4. After tMOD is satisfied (T145), any valid commands may be registered. (MR commands may already be issued after tMRD (T136).



Timing Details Write Leveling Exit

### 9.15. Multi Purpose Register(MR3)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.



- Pre-defined data pattern can be loaded into Multi Purpose Register (MPR) and read out by external read command.
- MR3 bit A2 defines dataflow from normal memory core or MPR. Once the dataflow is defined, the MPR contents can be continuously read out by regular READ or READ with Auto Precharge command.

#### Conceptual Block Diagram of Multi Purpose Register

To enable the MPR, a Mode Register Set (MRS) command must be issued to MR3 register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent READ or READA commands will be redirected to the multi purpose register. The resulting operation when a READ or READA command is issued is defined by MR3 bits [A1: A0] when the MPR is enabled. When the MPR is enabled, only READ or READA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2=0). Power-down mode, self-refresh, and any other non- READ/READA command are not allowed during MPR enable mode. The /RESET function is supported during MPR enable mode.

#### Functional Description of MR3 Bits for MPR

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See Table 13	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

Note: 1. See Available Data Locations and Burst Order Bit Mapping for Multi Purpose Register table

## 9.16. Read Operation

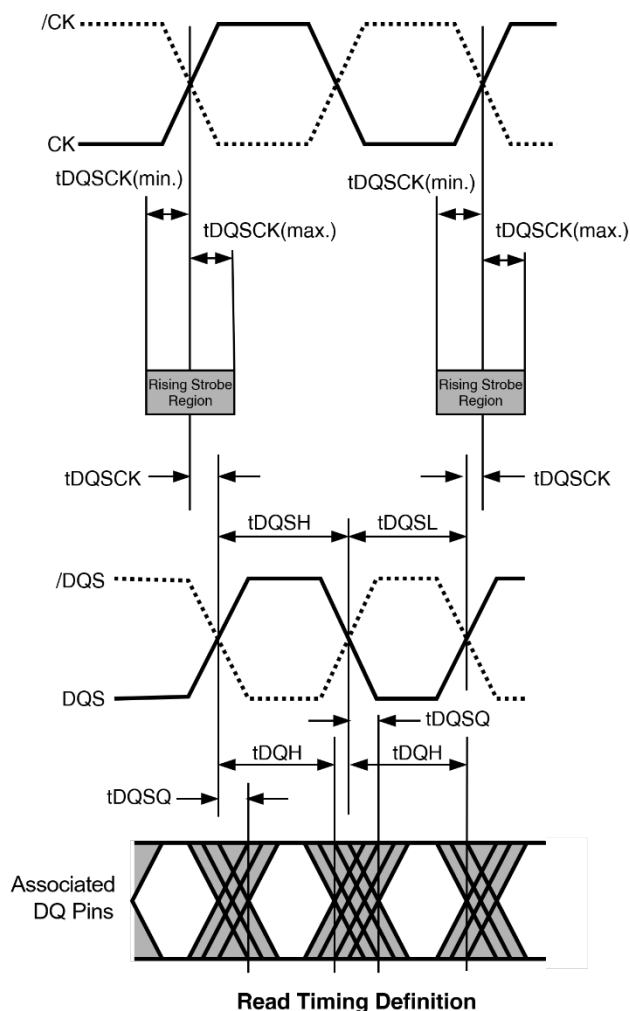
### 9.16.1. Read Timing Definition

Read timing is shown in the following Figure and is applied when the DLL is enabled and locked. Rising data strobe edge parameters:

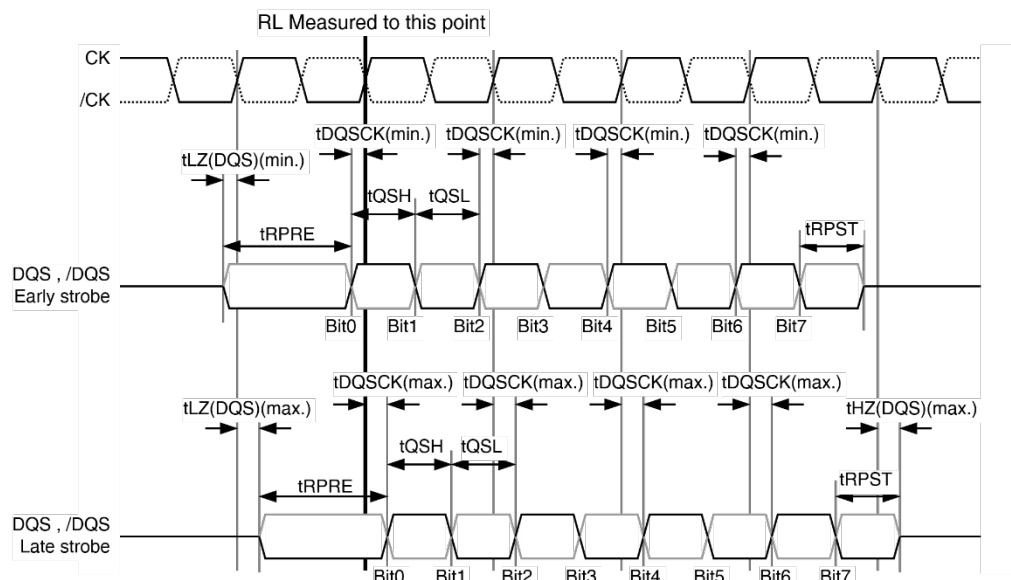
- $t_{DQSCK}$  min/max describes the allowed range for a rising data strobe edge relative to CK, /CK.
- $t_{DQSCK}$  is the actual position of a rising strobe edge relative to CK, /CK.
- $t_{QSH}$  describes the DQS, /DQS differential output high time.
- $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
- $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- $t_{QSL}$  describes the DQS, /DQS differential output low time.
  - $t_{DQSQ}$  describes the latest valid transition of the associated DQ pins.
  - $t_{QH}$  describes the earliest invalid transition of the associated DQ pins.
- $t_{DQSQ}$ ; both rising/falling edges of DQS, no tAC defined.



- CK, /CK crossing to DQS, /DQS crossing
- tDQSCK; rising edges only of CK and DQS
- tQSH; rising edges of DQS to falling edges of DQS
- tQSL; rising edges of /DQS to falling edges of /DQS
- tLZ (DQS), tHZ (DQS) for preamble/postamble (see tHZ (DQS), tLZ (DQS))



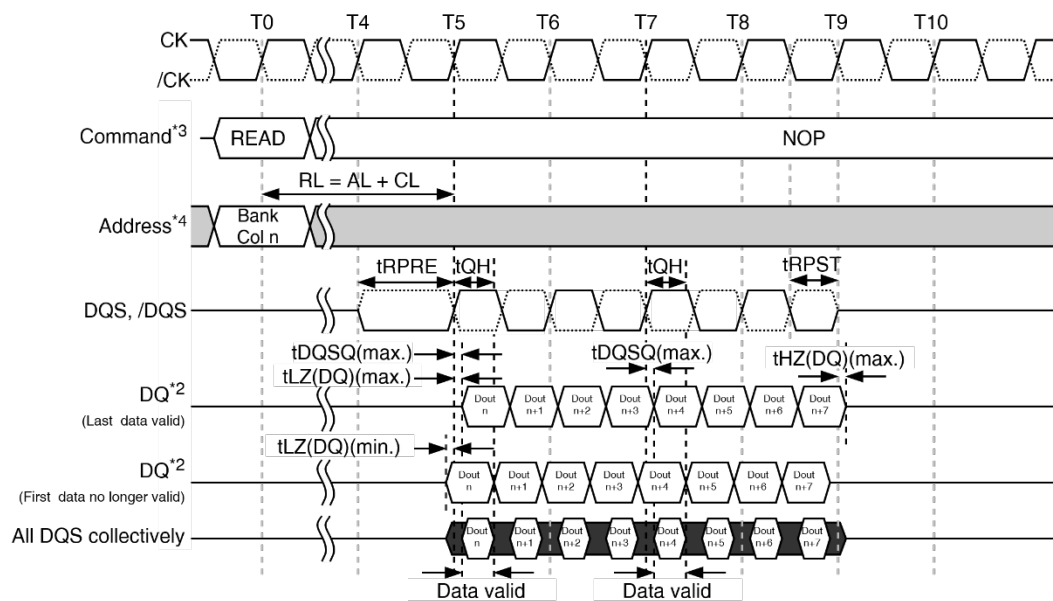
Notes:

1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK (min.) or tDQSCK(max.). Instead, rising strobe edge can vary between tDQSCK (min.) and tDQSCK (max.).
2. Notwithstanding note 1, a rising strobe edge with tDQSCK (max.) at T (n) can not be immediately followed by a rising strobe edge with tDQSCK (min.) at T (n+1). This is because other timing relationships (tQSH, tQSL) exist:  
if  $tDQSCK(n+1) < 0$ :  
 $tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - tDQSCK (n+1) |$
3. The DQS, /DQS differential output high time is defined by tQSH and the DQS, /DQS differential output low time is defined by tQSL.
4. Likewise, tLZ (DQS)min and tHZ (DQS)min are not tied to tDQSCKmin (earlystrobe case) and tLZ (DQS) max and tHZ (DQS) max are not tied to tDQSCKmax (late strobecase).
5. The minimum pulse width of read preamble is defined by tRPST (min.).
6. The maximum read postamble is bound by tDQSCK(min.) plus tQSH (min.) on the left side and tHZ(DQS)(max.) on the right side.
7. The minimum pulse width of read postamble is defined by tRPST (min.).
8. The maximum read preamble is bound by tLZ (DQS)(min.) on the left side and tDQSCK (max.) on the right side.

**DDR3 Clock to Data Strobe Relationship**



- DQS, /DQS crossing to Data Output
- tDQSQ; both rising/falling edges of DQS, no tAC defined



Notes:

1. BL8, RL = 5 (AL = 0, CL = 5).
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS, /DQS to data and does not define DQS, /DQS to clock.
7. Early data transitions may not always happen at the same DQ.  
Data transitions of a DQ can vary (either early or late) within a busy.

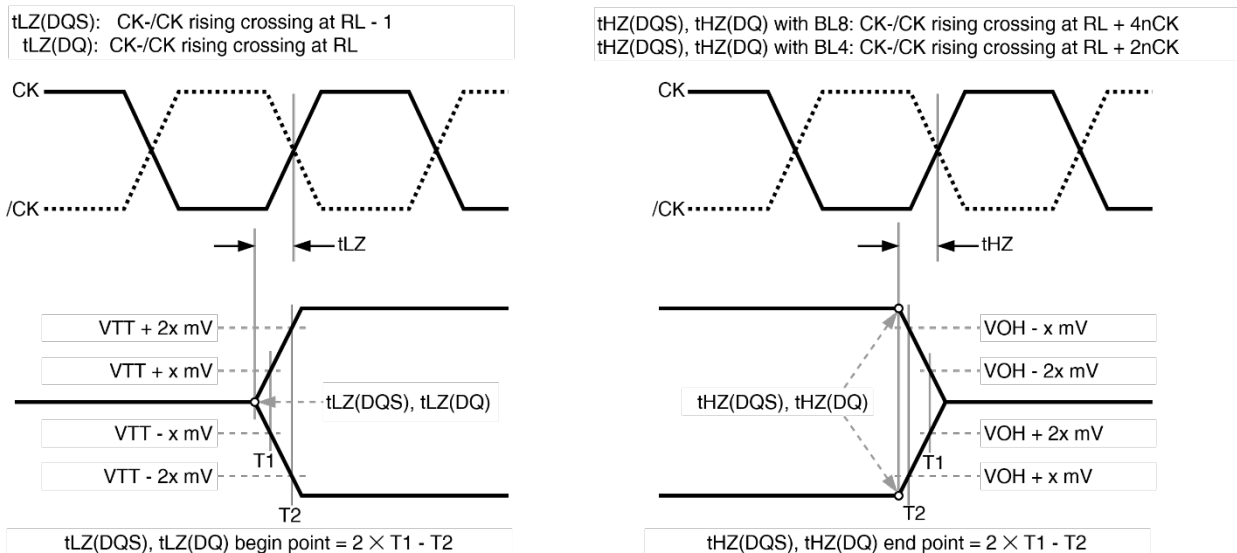
**DDR3 Data Strobe to Data Relationship**

### tLZ (DQS), tLZ (DQ), tHZ (DQS), tHZ (DQ) Notes

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). The figure below shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

### tRPRE Calculation

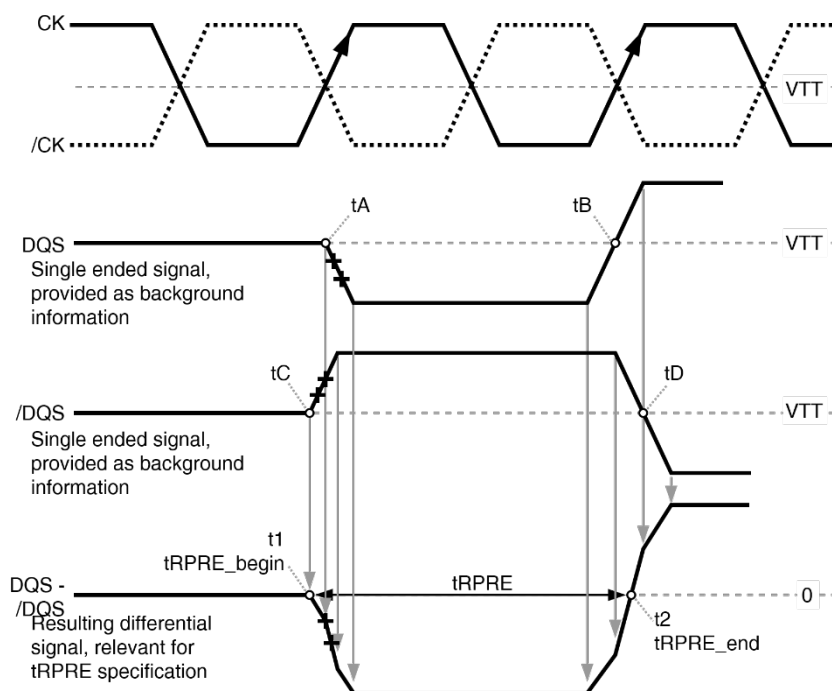
The method for calculating differential pulse widths for tRPRE is shown as follows.



### Method for Calculating Transitions and Endpoints

### tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown as follows.



### Method for Calculating tRPRE Transitions and Endpoint

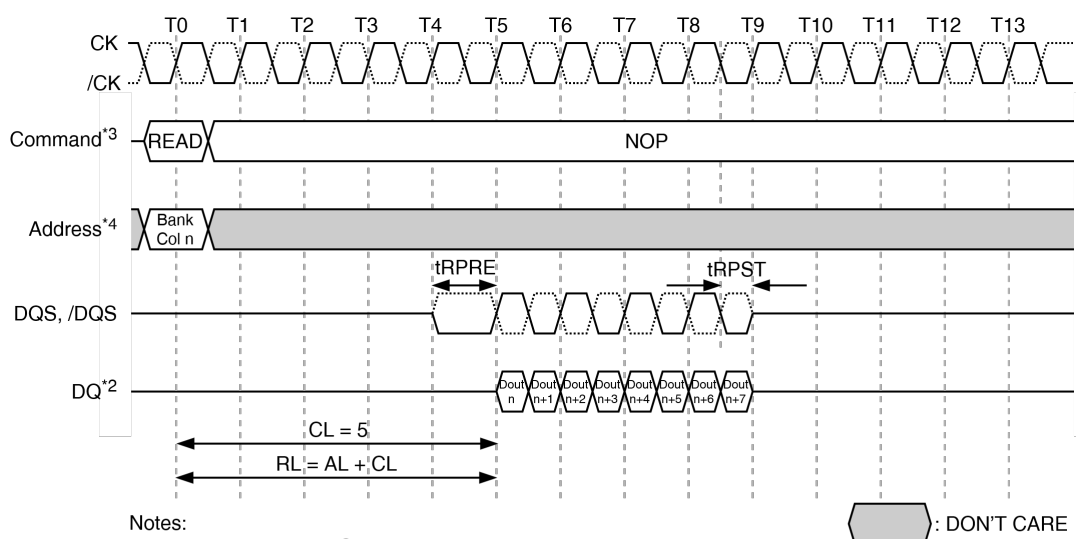
### 9.16.2. Read Operation

During read or write command DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (auto precharge can be enabled or disabled).

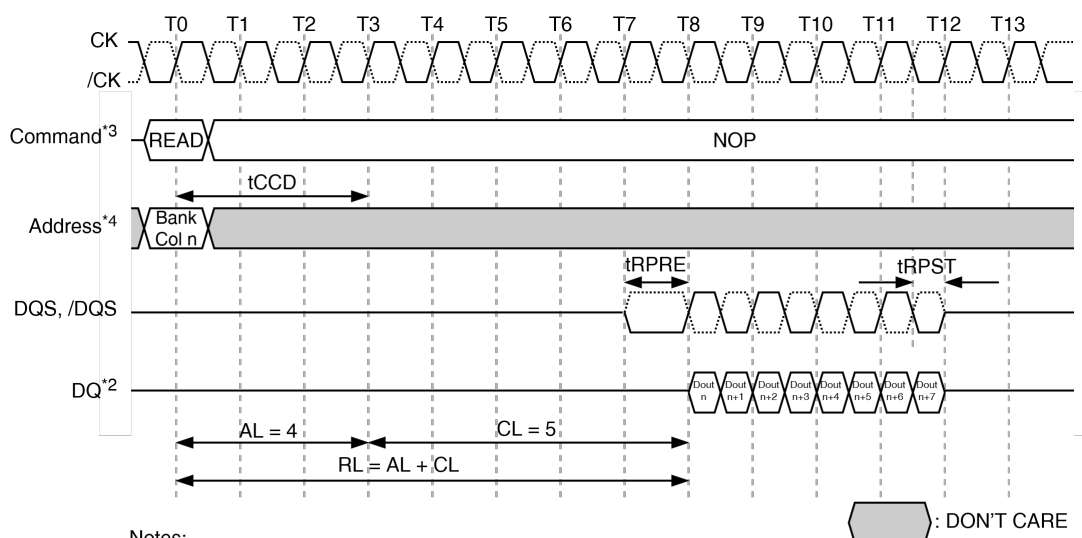
- A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
- A12 = 1, BL8

A12 will be used only for burst length control, not a column address.

The Burst Read command is initiated by having /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus /CAS latency (CL). The CL is defined by the Mode Register 0 (MR0), similar to the existing SDR and DDR-I SDRAMs. The AL is defined by the Mode Register 1



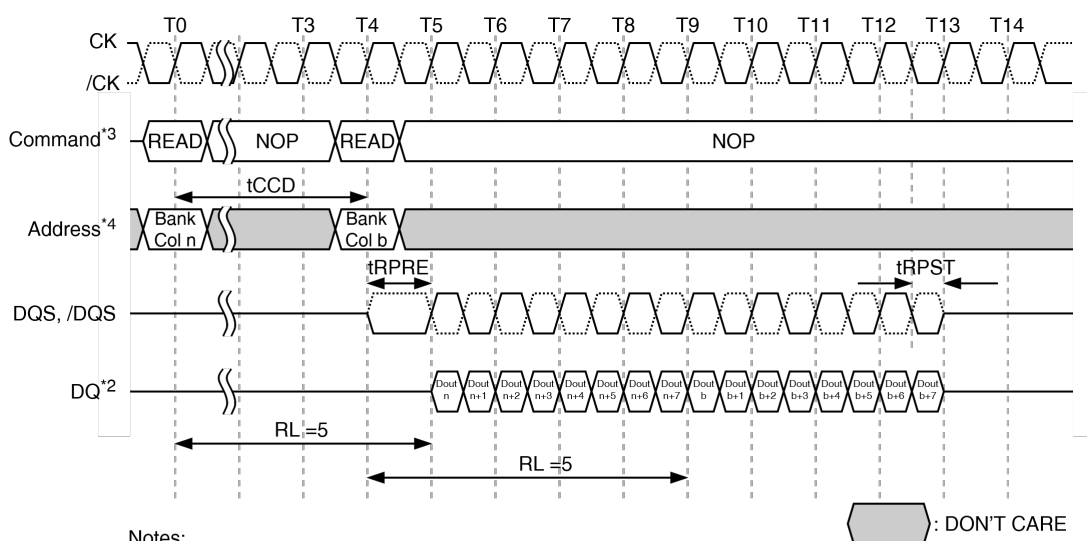
**Burst Read Operation, RL = 5**



Notes:

1. BL8, RL = 9, AL = (CL - 1), CL = 5
2. Dout n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

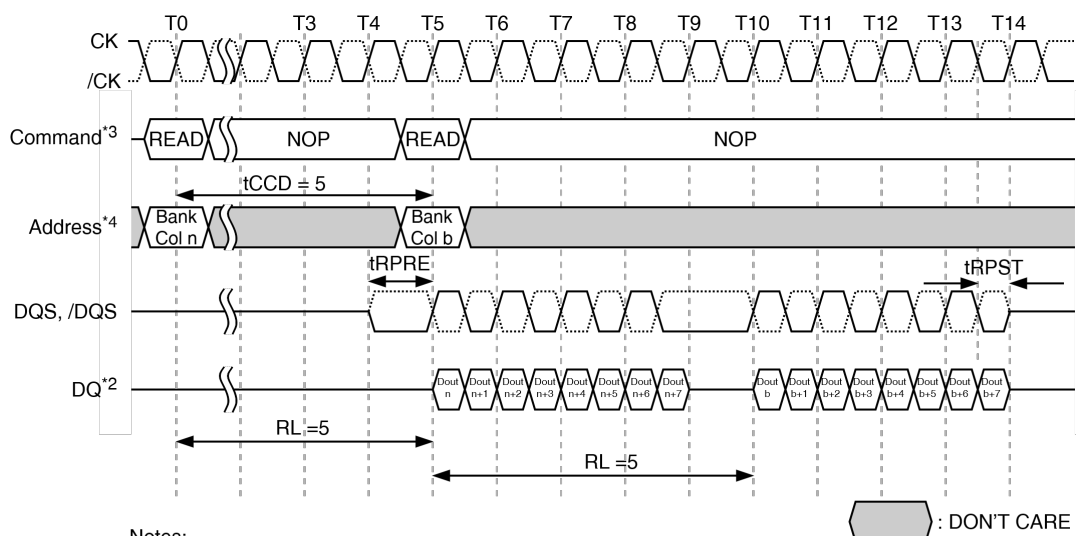
**Burst Read Operation, RL = 9**



Notes:

1. BL8, RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0 and T4.

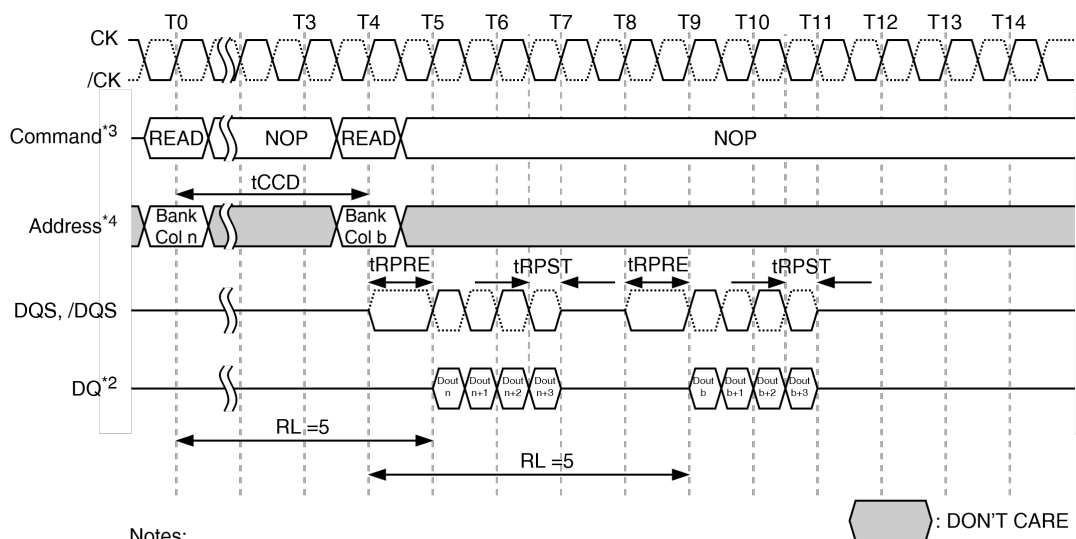
**Read (BL8) to Read (BL8)**



Notes:

1. BL8, RL = 5 (CL = 5, AL = 0), tCCD = 5.
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0 and T4.
5. DQS-/DQS is held logic low at T9.

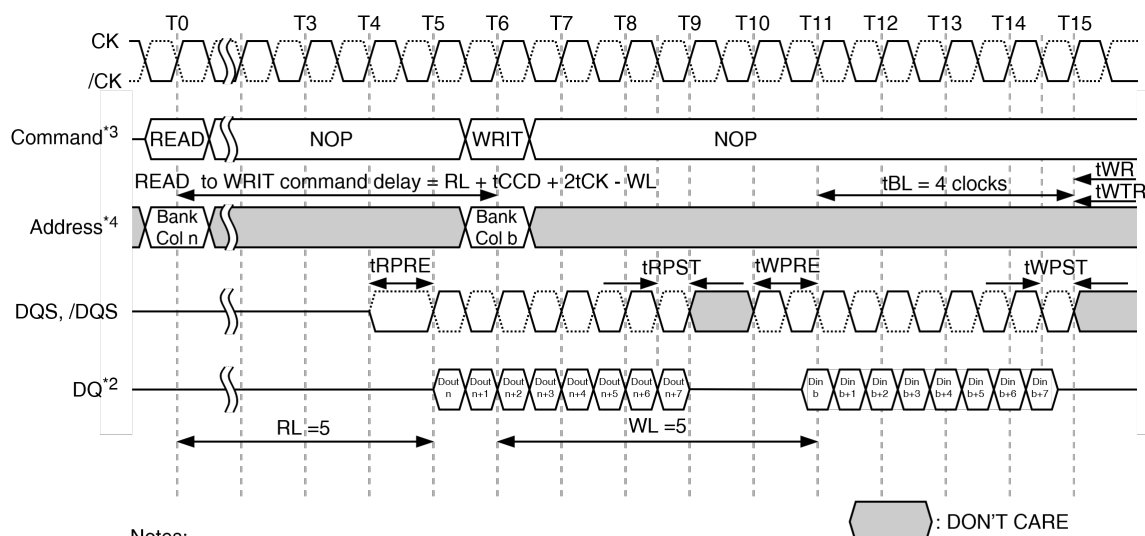
#### Nonconsecutive Read (BL8) to Read (BL8), tCCD = 5



Notes:

1. BC4, RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [1, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0 and T4.

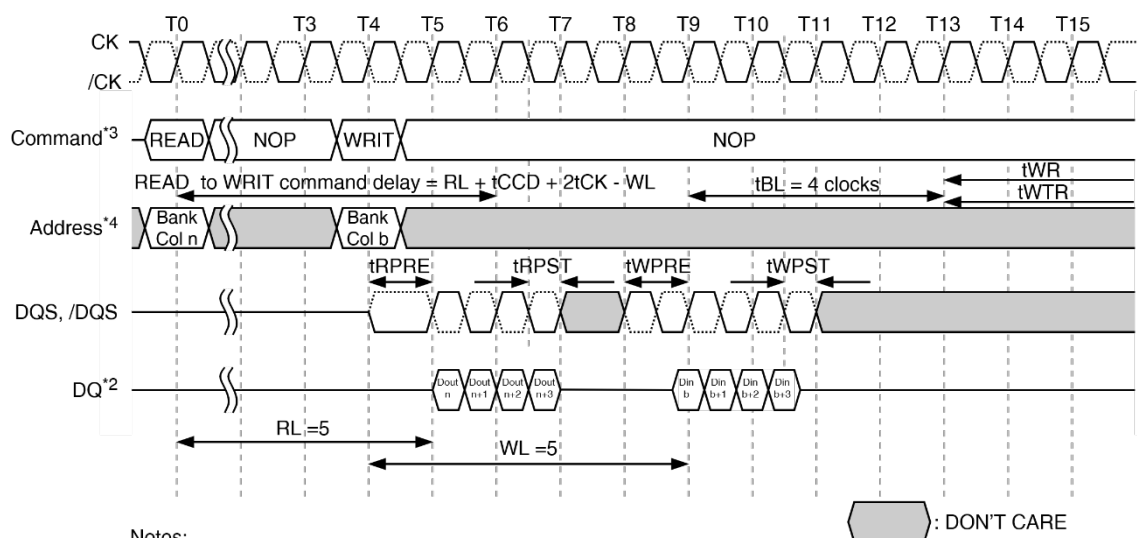
#### Read (BC4) to Read (BC4)



Notes:

1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0).
2. Dout n = data-out from column n, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0 and WRIT command T6.

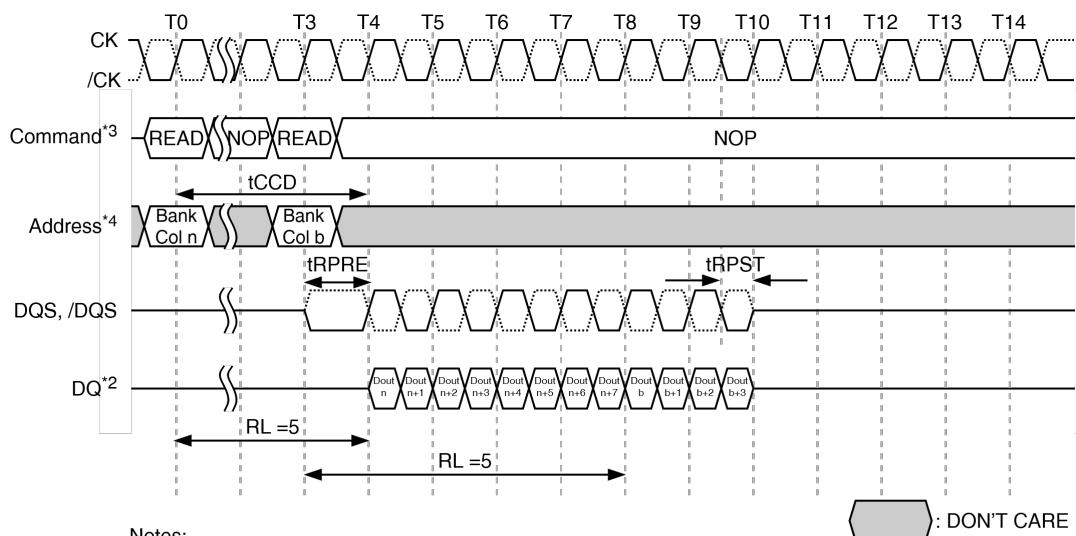
#### Read (BL8) to Write (BL8)



Notes:

1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0).
2. Dout n = data-out from column n, Din b= data-in from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0 and WRIT command T4.

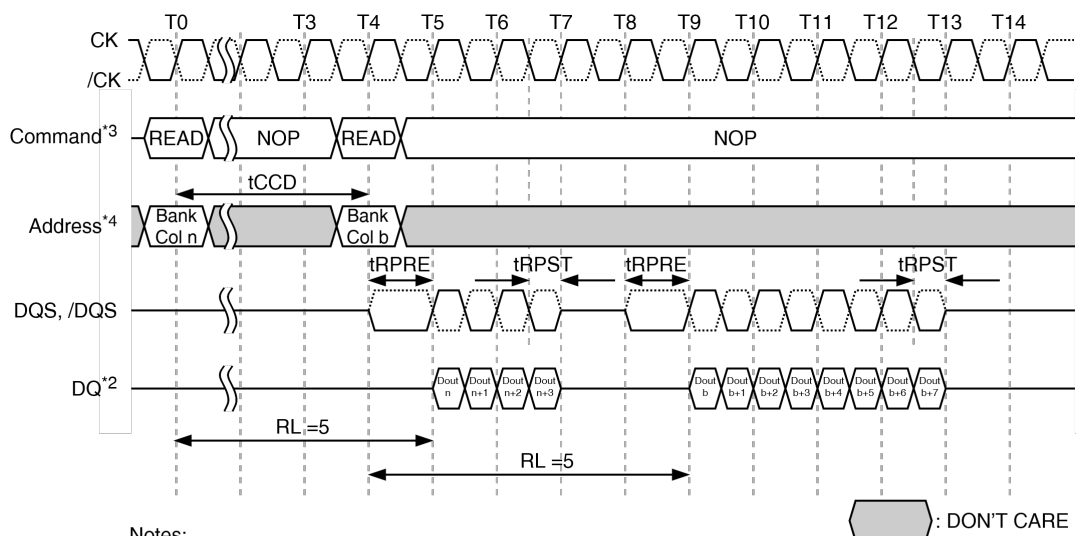
#### Read (BC4) to Write (BC4) OTF



Notes:

1. RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T4. BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T0.

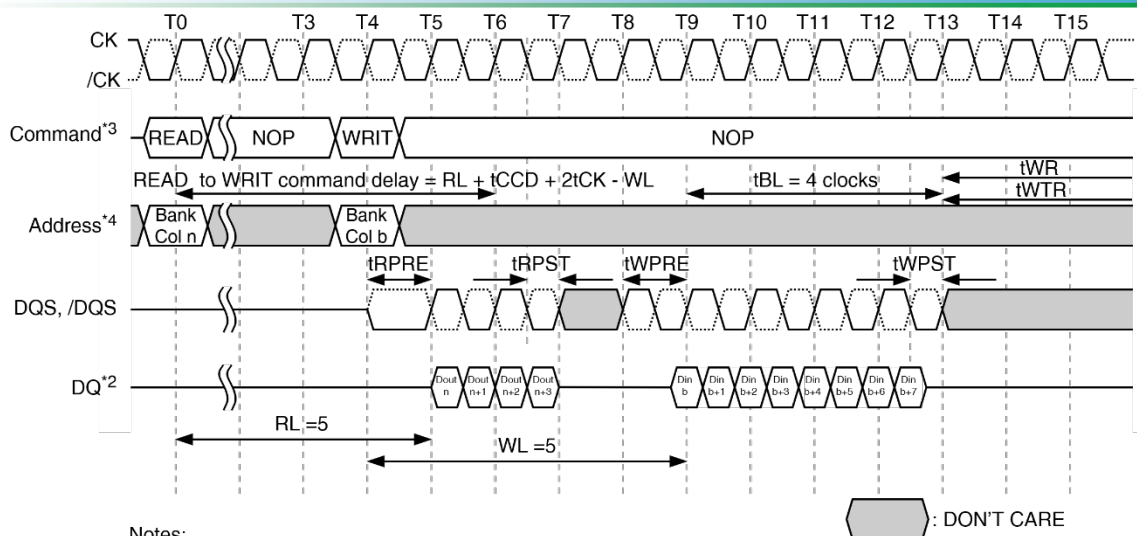
**Read (BL8) to Read (BC4) OTF**



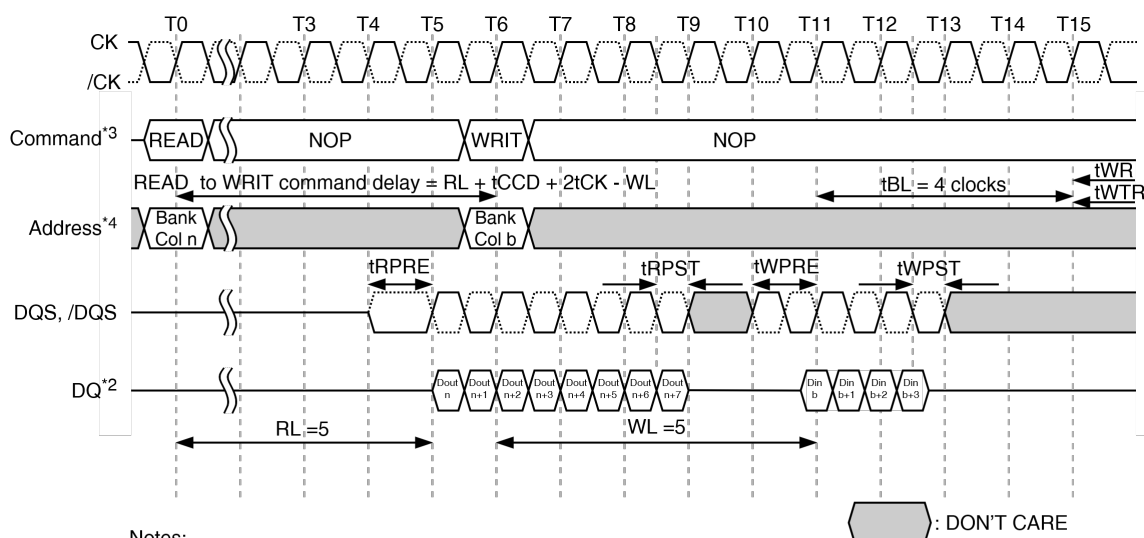
Notes:

1. RL = 5 (CL = 5, AL = 0).
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during READ command at T0. BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during READ command at T4.

**Read (BC4) Read (BL8) OTF**

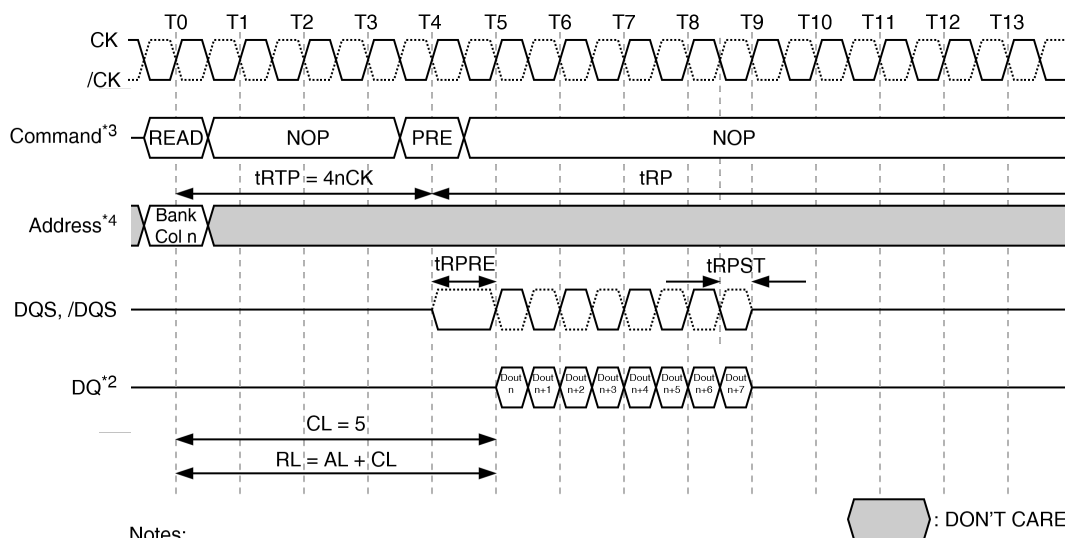


### Read (BC4) to Write (BL8) OTF

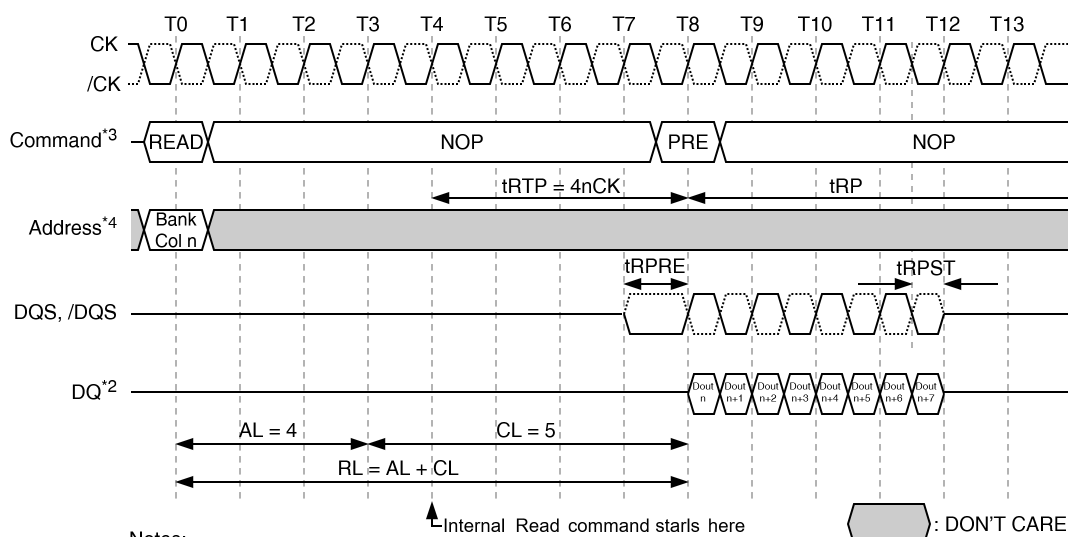


### Read (BL8) to Write (BC4) OTF





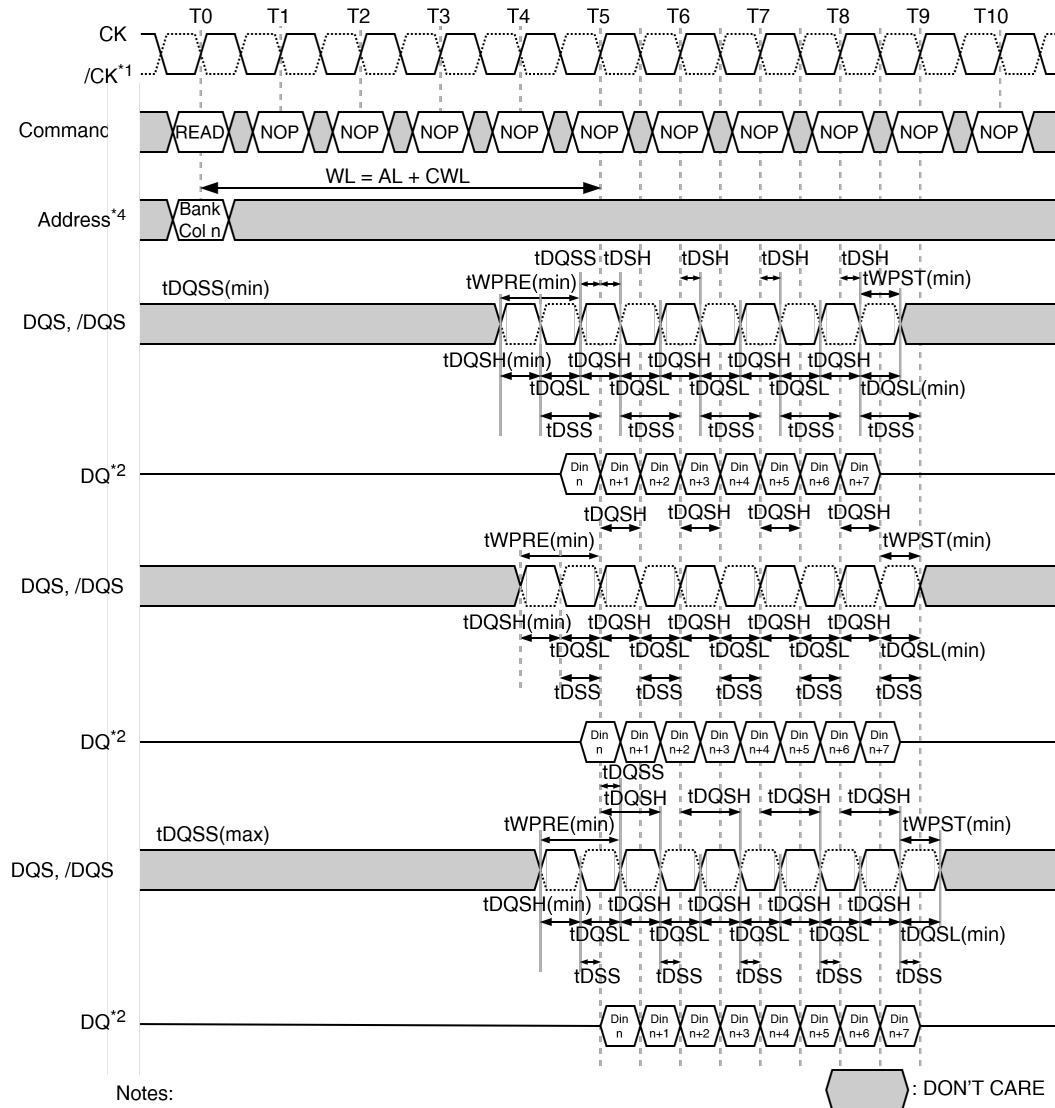
#### Burst Read Precharge Operation, RL = 5



#### Burst Read Precharge Operation, RL = 9

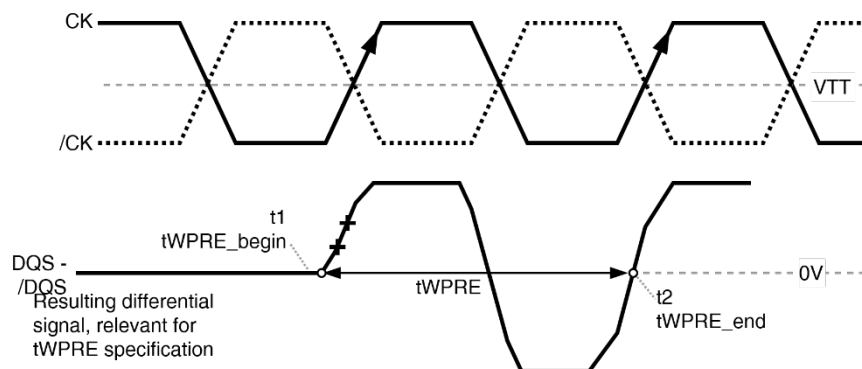
## 9.17. Write Operation

### 9.17.1. Write Timing Definition

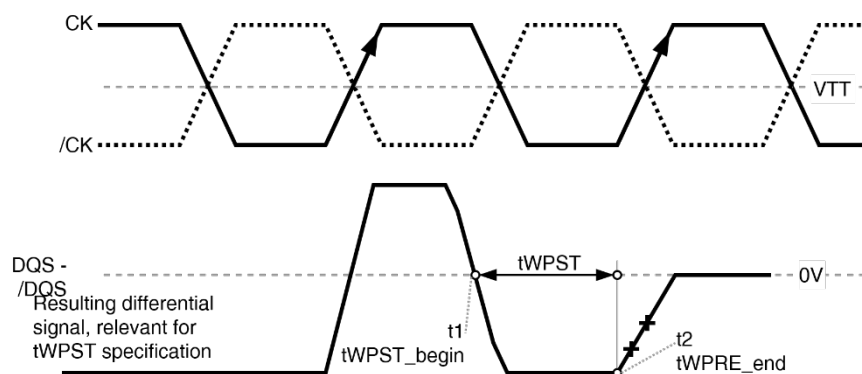


#### tWPRE Calculation

The method for calculating differential pulse widths for tWPRE is shown as follows.



#### Method for Calculating tWPRE Transitions and Endpoints



#### Method for Calculating tWPST Transitions and Endpoints

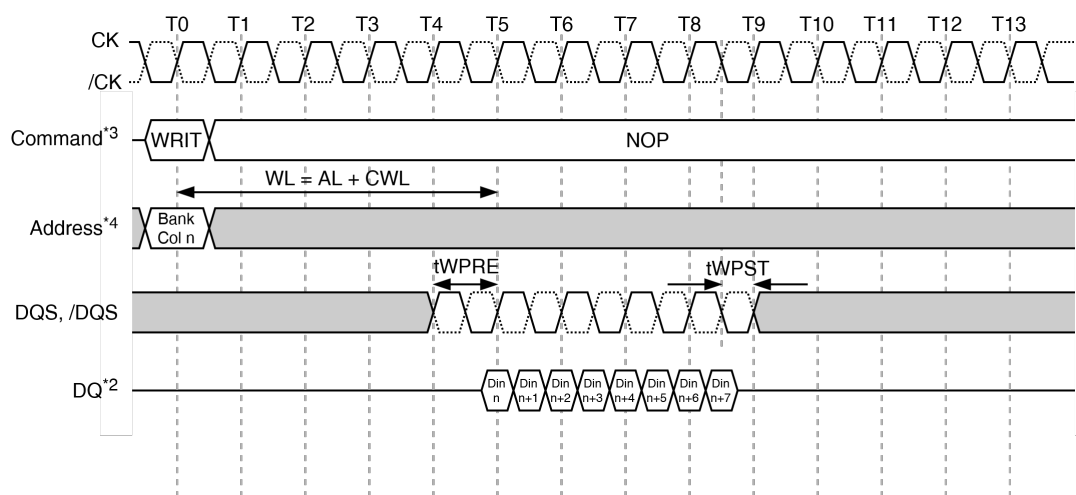
### 9.17.2. Write Operation

During read or write command DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (auto precharge can be enabled or disabled).

- A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
- A12 = 1, BL8

A12 will be used only for burst length control, not a column address.

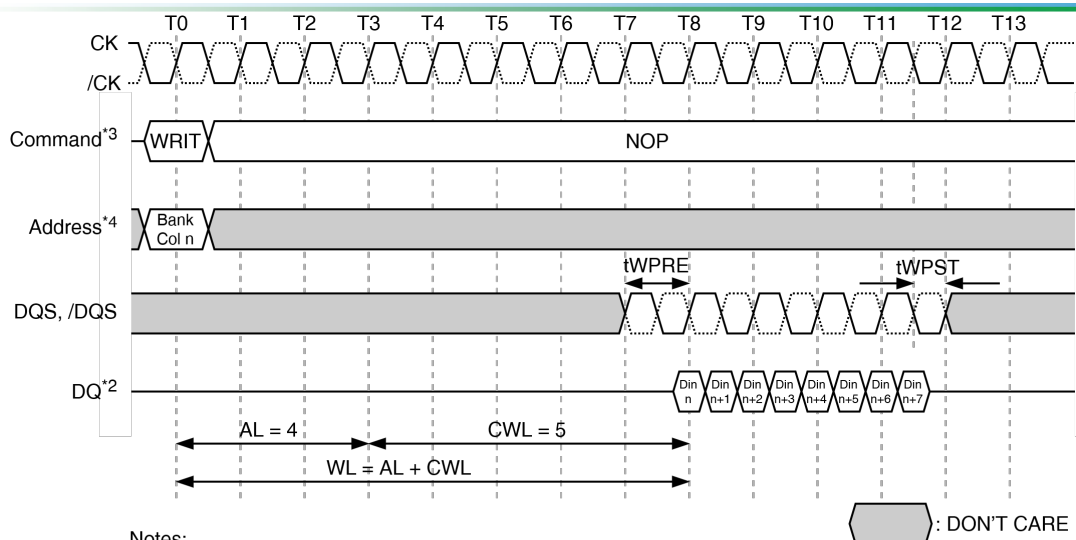
The Burst Write command is initiated by having /CS, /CAS and /WE low while holding /RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is equal to (AL + CWL). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length of 4 is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (tWR).



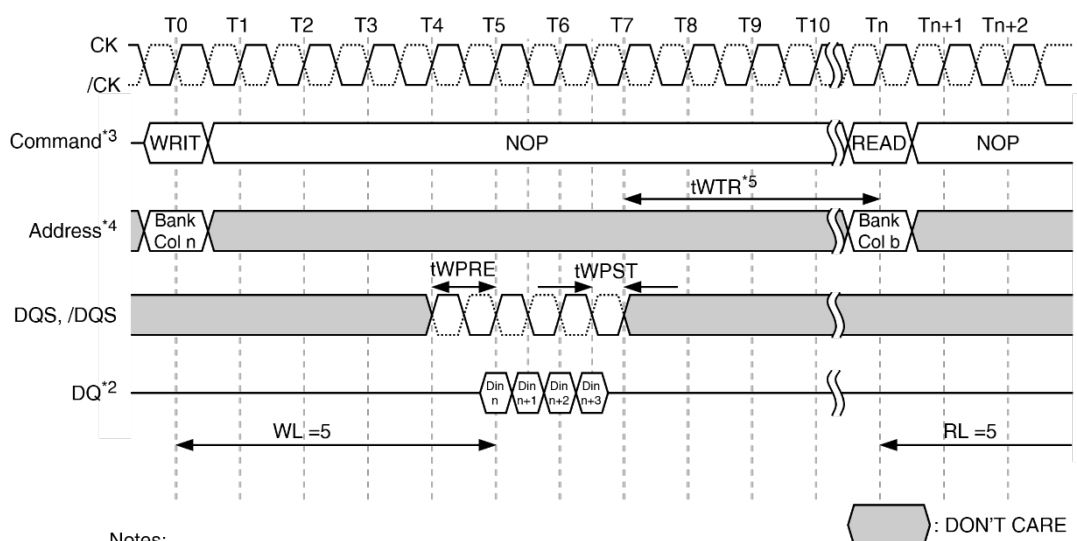
Notes:

1. BL8, WL = 5 (AL = 0, CWL = 5)
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.

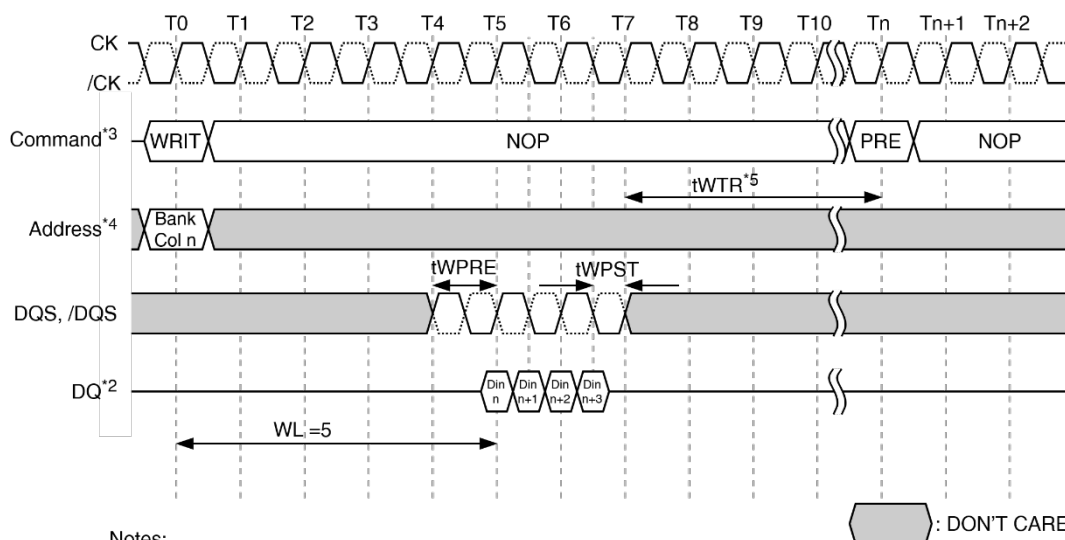
#### Burst Write Operation, WL = 5



### Burst Write Operation, WL = 9



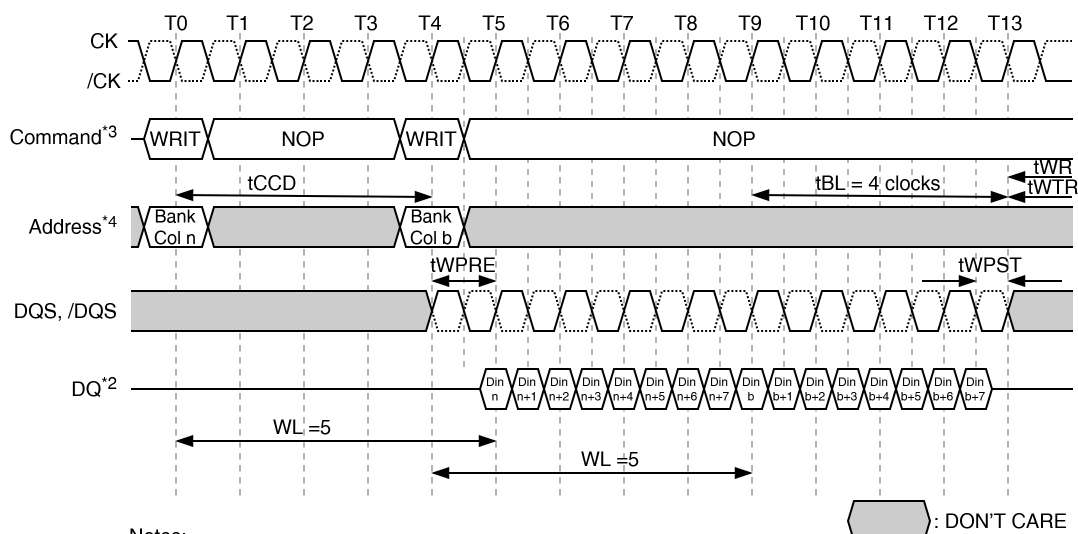
### Write (BC4) to Read (BC4) Operation



Notes:

1. BC4, WL = 5, RL = 5.
2. Din n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [1, 0] during WRIT command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7. tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

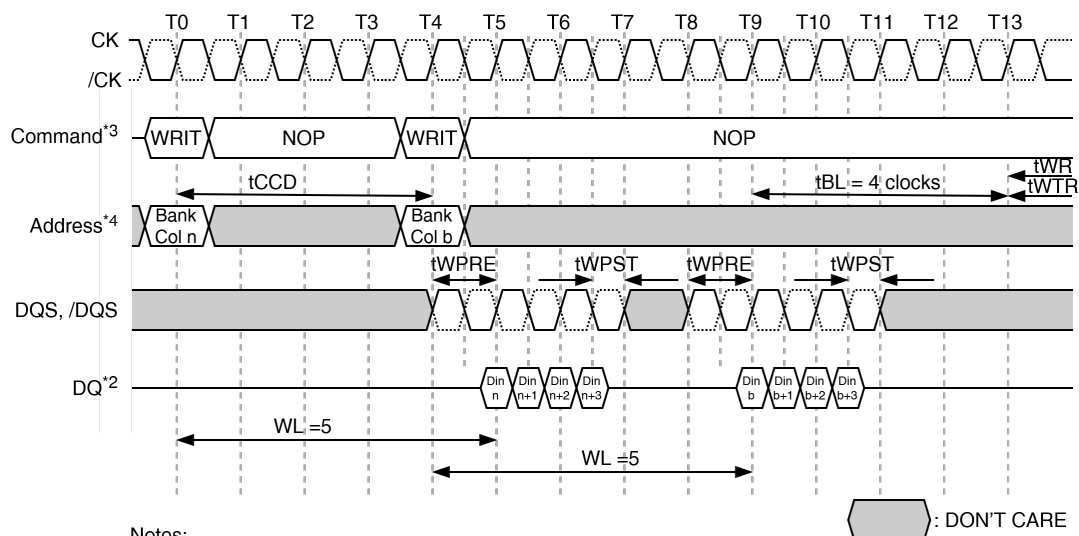
#### Write (BC4) to Precharge Operation



Notes:

1. BL8, WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0 and T4.

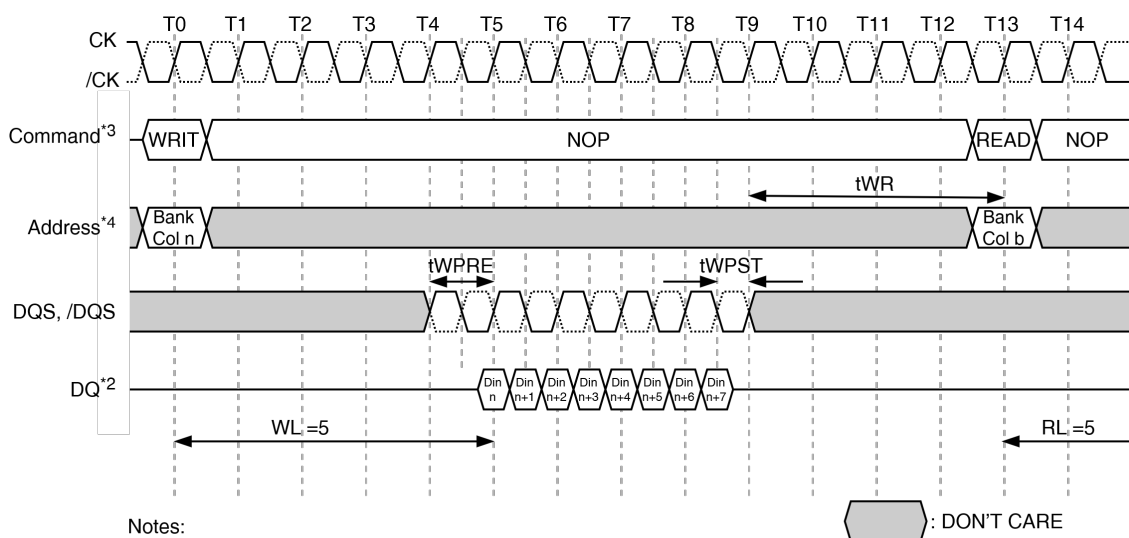
#### Write (BL8) to Write (BL8) OTF



Notes:

1. BC4, WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T0 and T4.

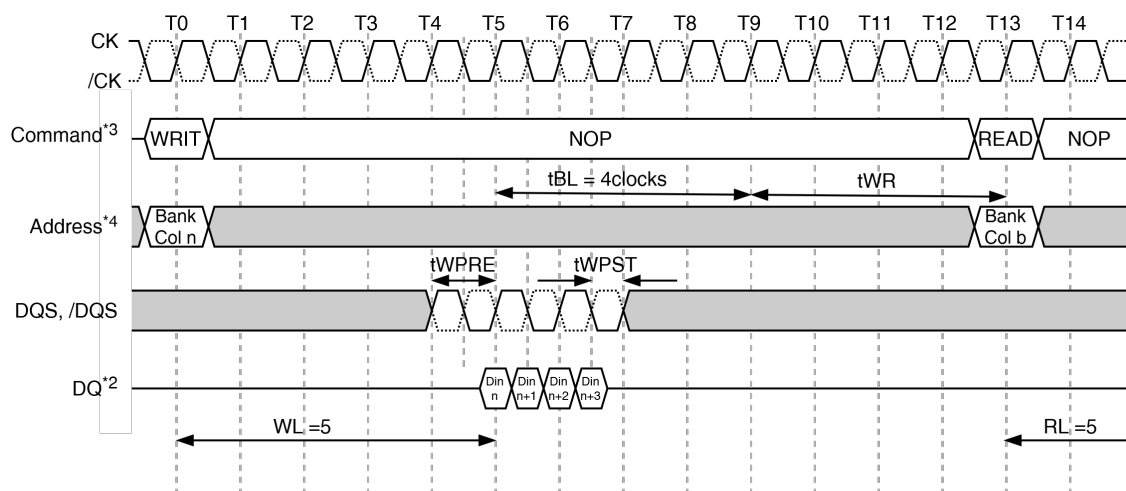
#### Write (BC4) to Write (BC4) OTF



Notes:

1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Din n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 0] or MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.  
READ command at T13 can be either BC4 or BL8 depending on MR0 bit [A1, A0] and A12 status at T13.

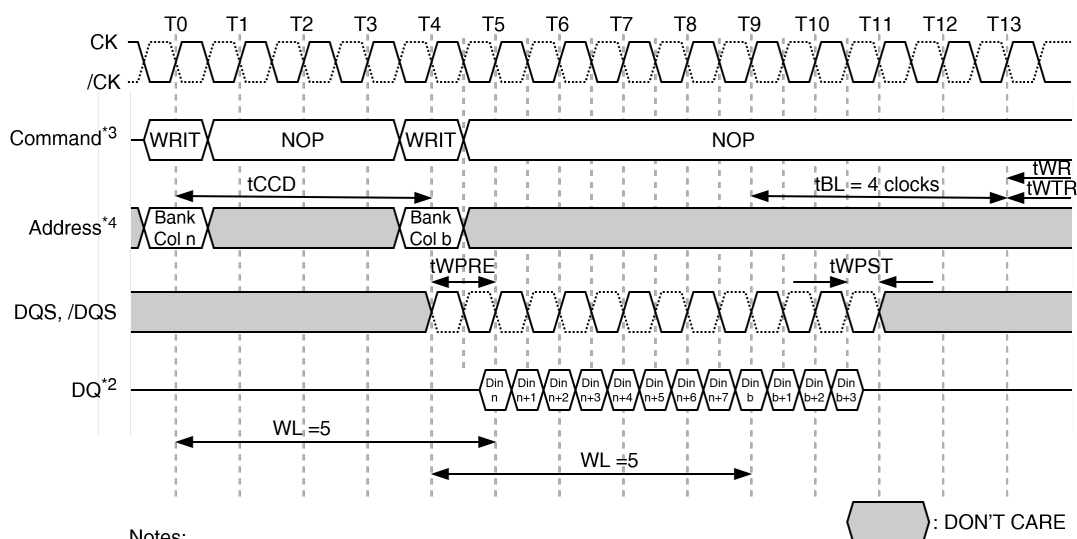
#### Write (BL8) to Read (BC4/BL8) OTF



Notes:

1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Din n = data-in from column n; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T0.  
READ command at T13 can be either BC4 or BL8 depending on MR0 bit [A1, A0] and A12 status at T13.

**Write (BC4) to Read (BC4/BL8) OTF**

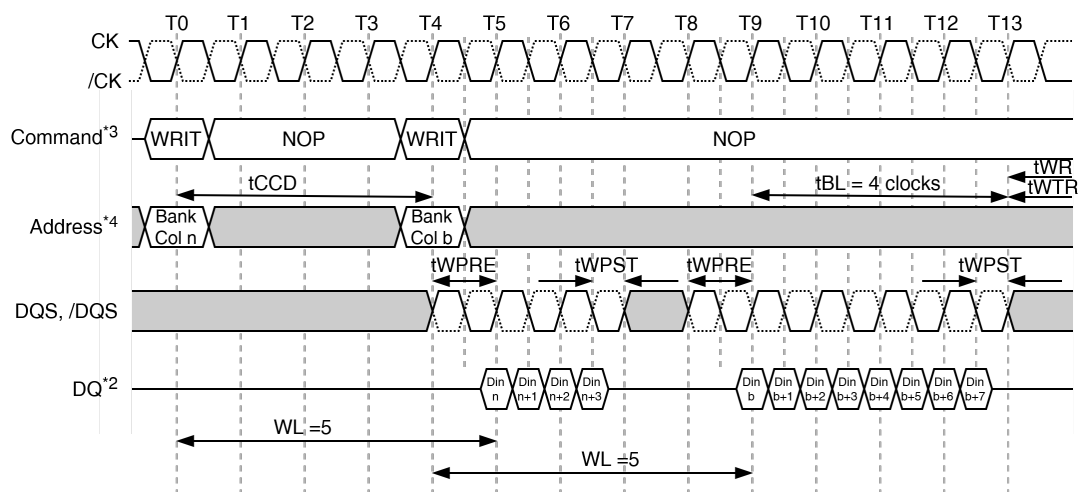


Notes:

1. WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T0.  
BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T4.

**Write (BL8) to Write (BC4) OTF**





Notes:

1. WL = 5 (CWL = 5, AL = 0)
2. Din n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 0 during WRIT command at T0.  
BL8 setting activated by MR0 bit [A1, A0] = [0, 1] and A12 = 1 during WRIT command at T4.

**Write (BC4) to Write (BL8) OTF**

### 9.17.3. Write Timing Violations

#### Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly.

However, it is desirable for certain minor violations, that the DRAM is guaranteed not to "hang up" and error to be limited to that particular operation.

For the following it will be assumed that there are no timing violations w.r.t to the write command itself (including ODT etc.) and that it does satisfy all timing requirements not mentioned below.

#### Data Setup and Hold Violations

Should the data to strobe timing requirements ( $t_{DS}$ ,  $t_{DH}$ ) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this write command.

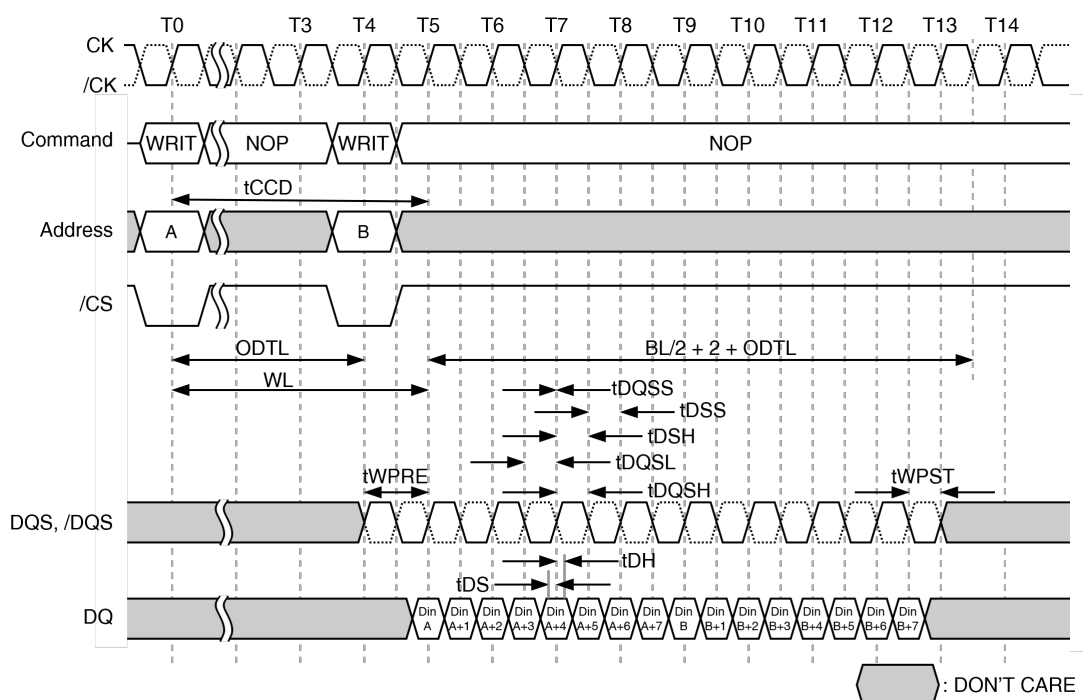
In the example (Figure Write Timing Parameters) the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

#### Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements ( $t_{DQSH}$ ,  $t_{DQSL}$ ,  $t_{WPRE}$ ,  $t_{WPST}$ ) or the strobe to clock timing requirements ( $t_{DSS}$ ,  $t_{DSH}$ ,  $t_{DQSS}$ ) be violated for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with the offending write command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

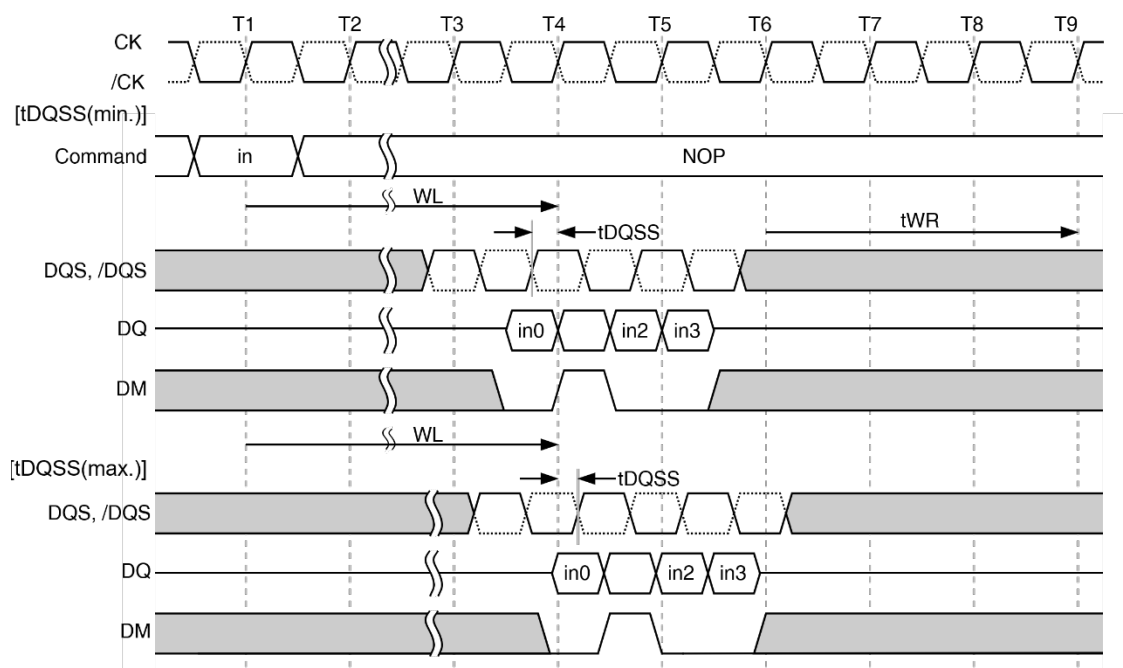
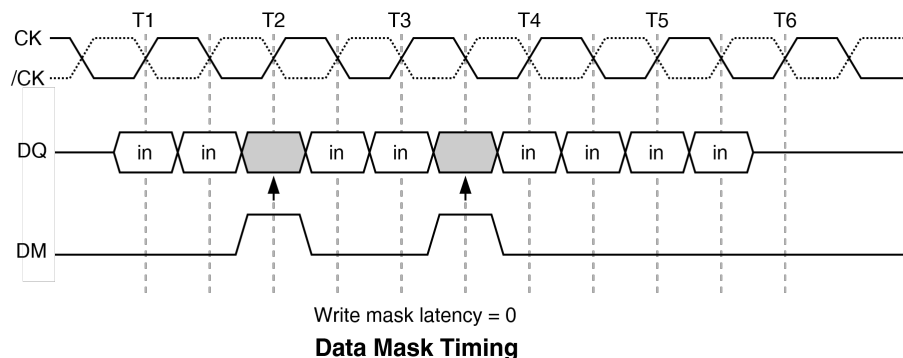
In the example (Figure Write (BL8) to Write (BL8) OTF) the relevant strobe edges for write burst n are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting and ending on one of these strobe edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.



Write Timing Parameters

### Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR3 SDRAMs, Consistent with the implementation on DDR-I SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles.



### 9.18. Power-Down Modes

Power-down is synchronously entered when CKE is registered low (along with NOP or DESL command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode; if any bank is open after in-progress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK, /CK, ODT, CKE and /RESET. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or DESL commands are needed during the CKE switch off and cycle(s) after this timing period are defined as tCPDED. CKE\_low will result in deactivation of command and address receivers after tCPDED has expired.

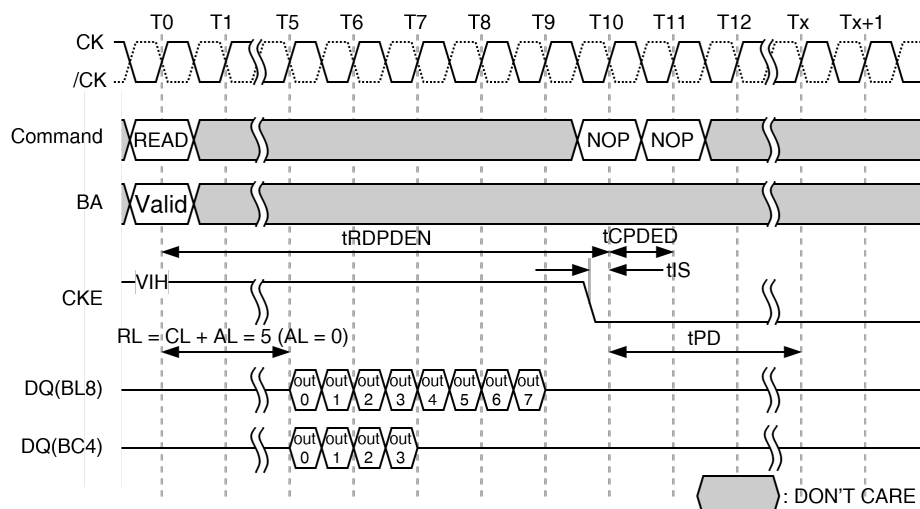
[Power-Down Entry Definitions]

Status of DRAM	MR0 bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more open)	Don't Care	On	Fast	tXP to any valid command
Precharged (All banks precharged)	0	Off	Slow	tXP to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS, PRE or PALL. tXPDLL to commands who need DLL to operate, such as READ, READA or ODT control line.
Precharged (All banks precharged)	1	On	Fast	tXP to any valid command

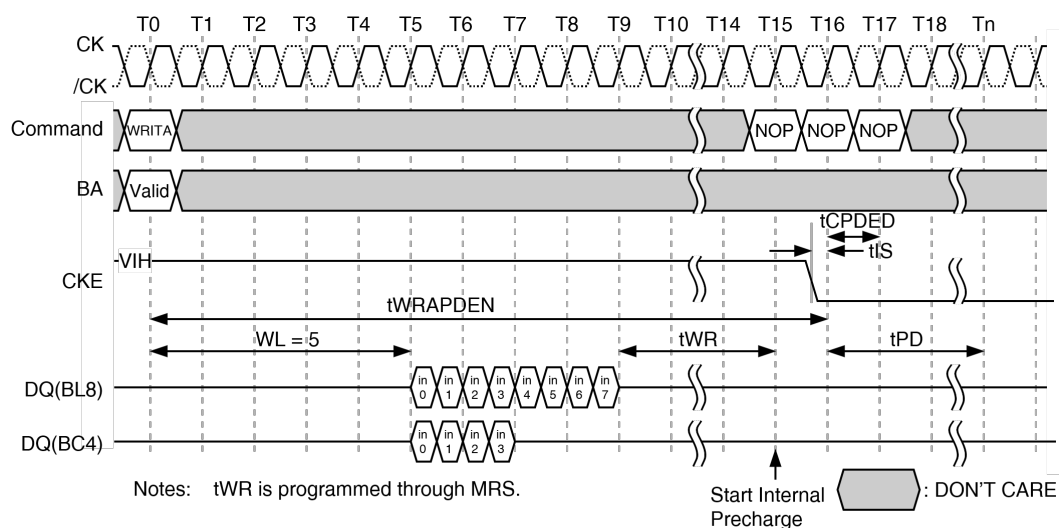
Also, the DLL is disabled upon entering precharge power-down for slow exit mode, but the DLL is kept enabled during precharge power-down for fast exit mode or active power-down. In power-down mode, CKE low, RESET high and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care" (If RESET goes low during power-down, the DRAM will be out of PD mode and into reset state). CKE low must be maintained until tPD has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or DESL command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined at AC Characteristics table of this data sheet.

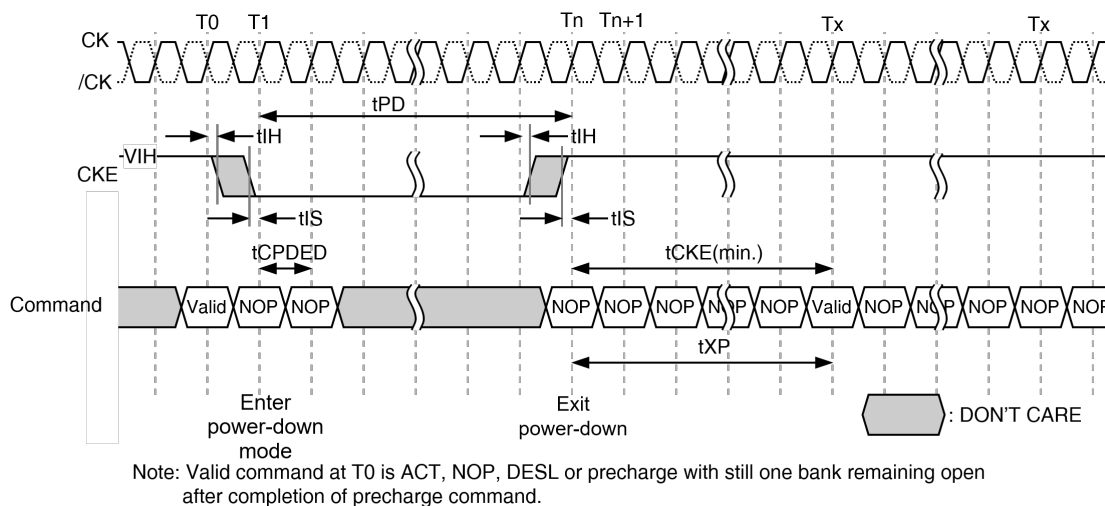
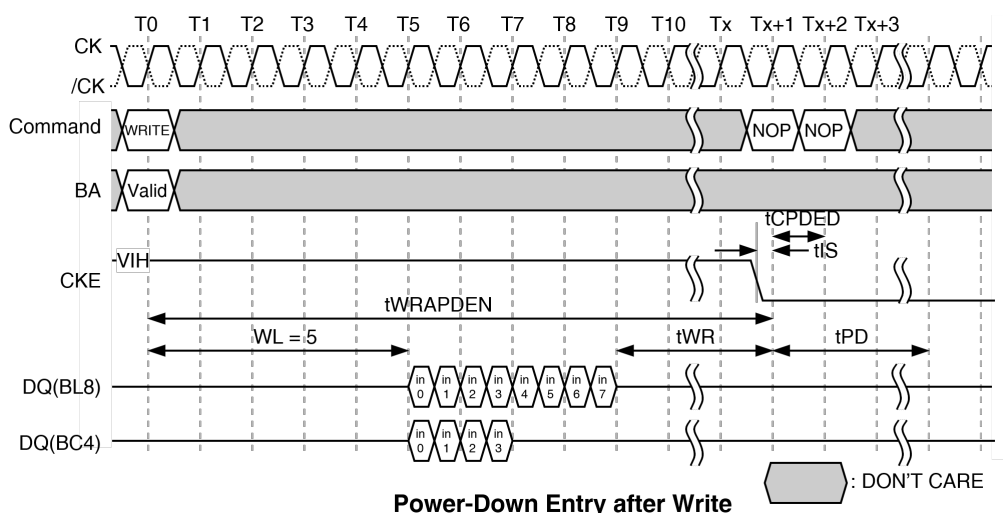
### 9.18.1. Timing Diagrams for Proposed CKE with Power-Down Entry, Power-Down Exit



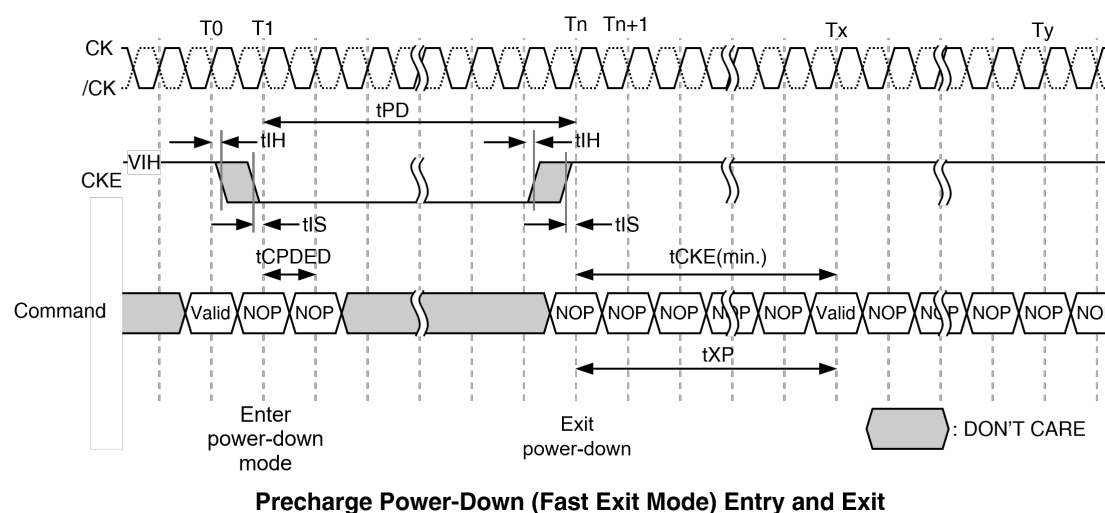
**Power-Down Entry after Read and Read with Auto Precharge**

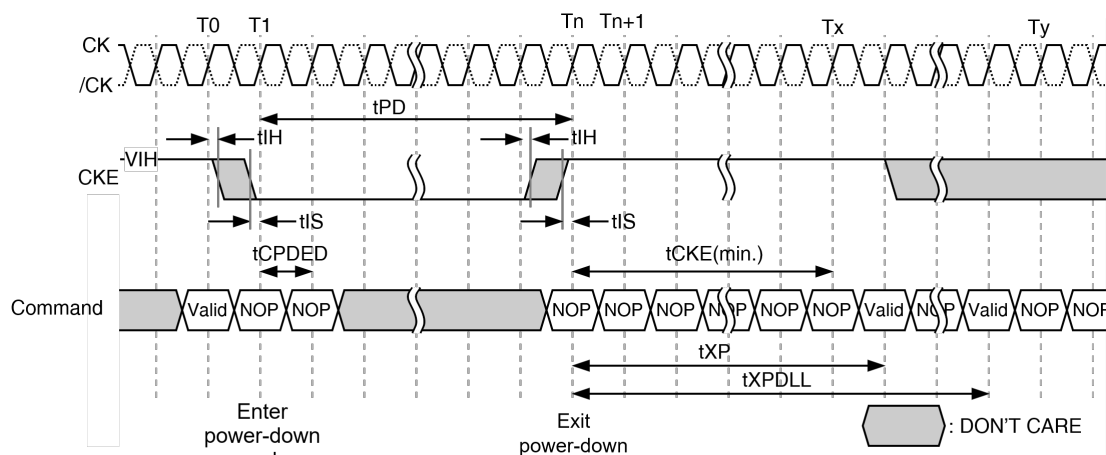


**Power-Down Entry After Write with Auto Precharge**

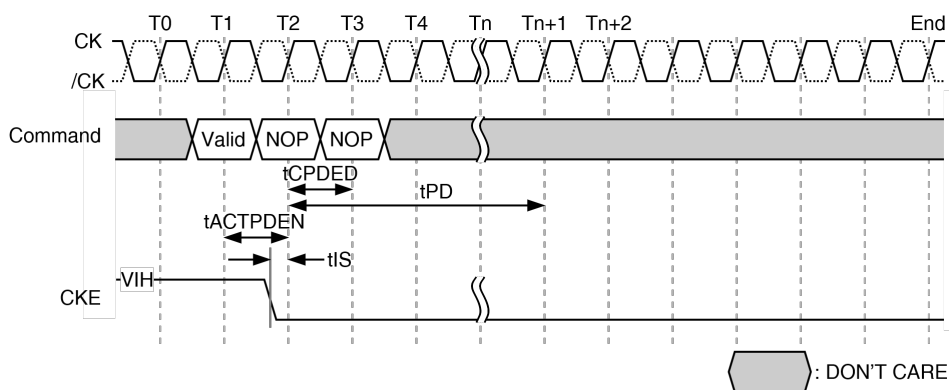


Note: Valid command at T0 is ACT, NOP, DESL or precharge with still one bank remaining open after completion of precharge command.

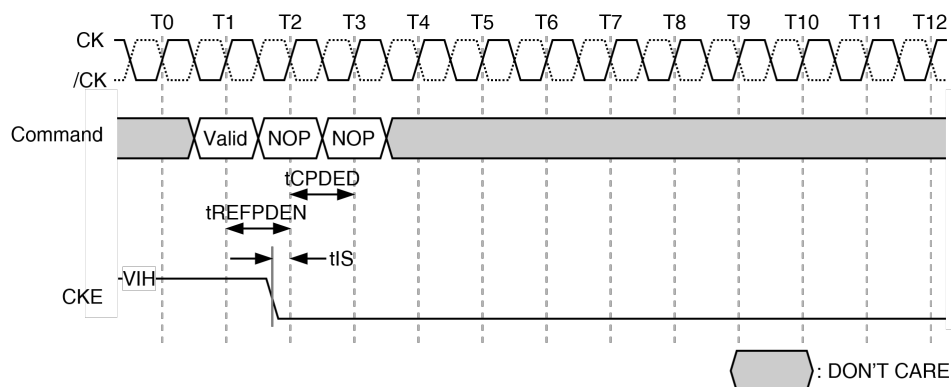




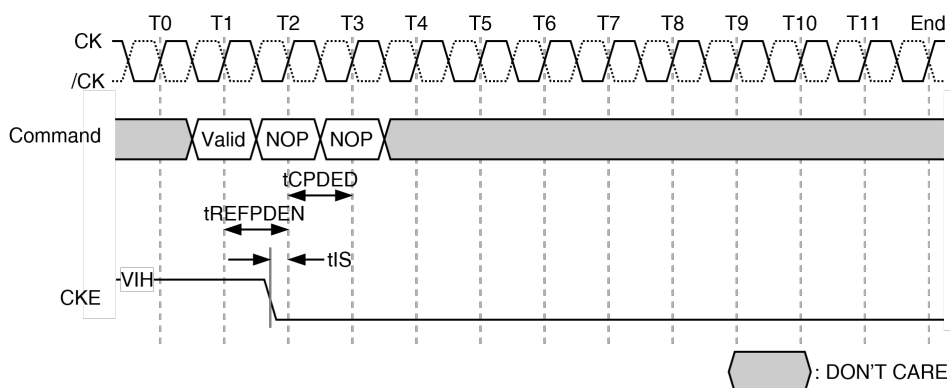
**Precharge Power-Down (Slow Exit Mode) Entry and Exit**



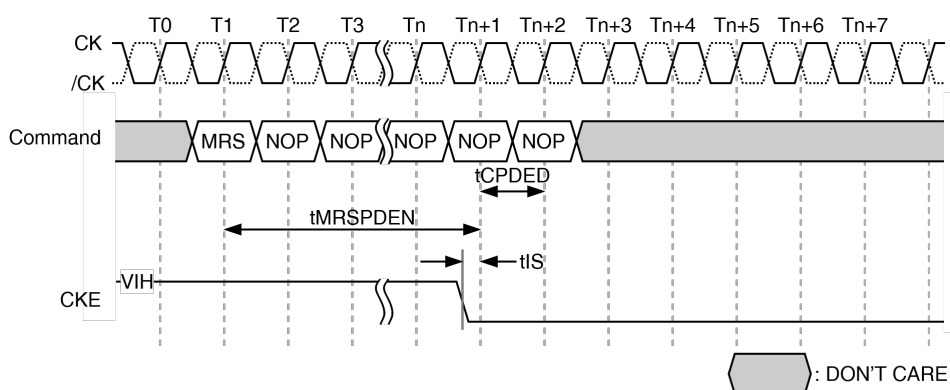
**Active Command to Power-Down Entry**



**Refresh Command to Power-Down Entry**



**Precharge/Precharge All Command to Power-Down Entry**



**MRS Command to Power-Down Entry**



### 9.18.2. Timing Values tXXPDEN Parameters

Status of DRAM	Last Command before CKE_low	Parameter	Parameter Value	Unit
Idle or Active	Activate	tACTPDEN	1	nCK
Idle or Active	Precharge	tPRPDEN	1	nCK
Active	READ/READA	tRDPDEN	RL + 4 + 1	nCK
Active	WRIT for BL8MRS, BL8OTF, BC4OTF	tWRPDEN	WL + 4 + (tWR/tCK (avg)) <sup>*1</sup>	nCK
Active	WRIT for BC4MRS	tWRPDEN	WL + 2 + (tWR/tCK (avg)) <sup>*1</sup>	nCK
Active	WRITA for BL8MRS, BL8OTF, BC4OTF	tWRAPDEN	WL + 4 + WR <sup>*2</sup> + 1	nCK
Active	WRITA for BC4MRS	tWRAPDEN	WL + 2 + WR <sup>*2</sup> + 1	nCK
Idle	Refresh	tREFPDEN	1	nCK
Idle	Mode Register Set	tREFPDEN	tMOD	

Notes: 1. tWR is defined in ns, for calculation of tWRPDEN, it is necessary to round up tWR / tCK to next integer.  
2. WR in clock cycles as programmed in mode register.

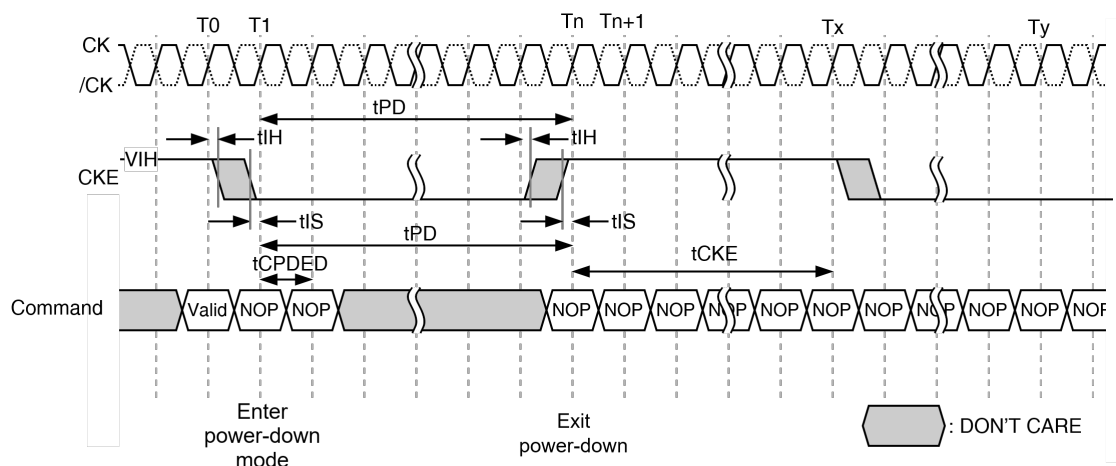
### 9.18.3. Power-Down Entry and Exit Clarification

Case 1:

When CKE registered low for power-down entry, tPD must be satisfied before CKE can be registered high for power-down exit.

Case 1a:

After power-down exit, tCKE must be satisfied before CKE can be registered low again.



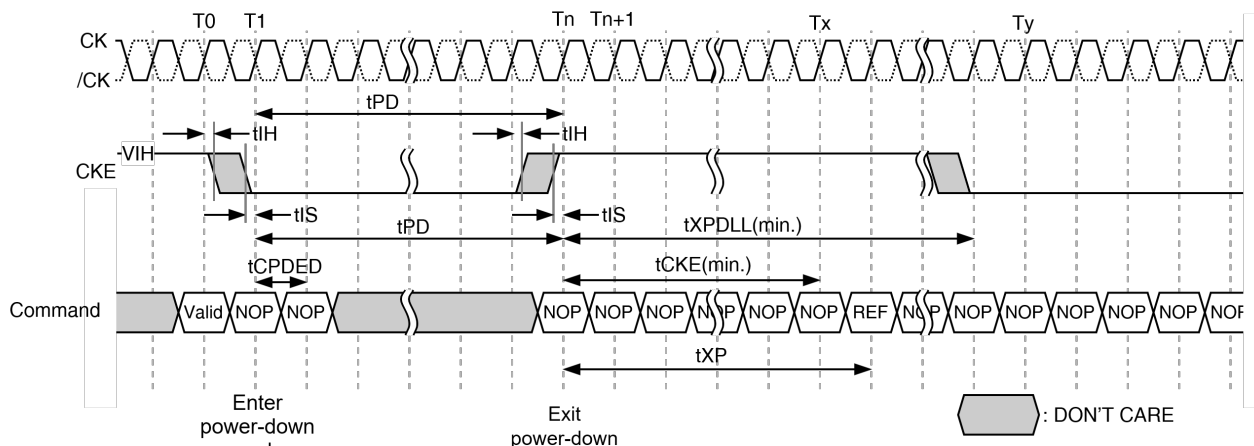
Power-Down Entry/Exit Clarifications (1)

#### Case 2:

For certain CKE intensive operations, for example, repeated "PD Exit - Refresh - PD Entry" sequence, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore the following conditions must be met in addition to  $t_{PD}$  in order to maintain proper DRAM operation when Refresh commands is issued in between PD Exit and PD Entry.

Power-down mode can be used in conjunction with Refresh command if the following conditions are met:

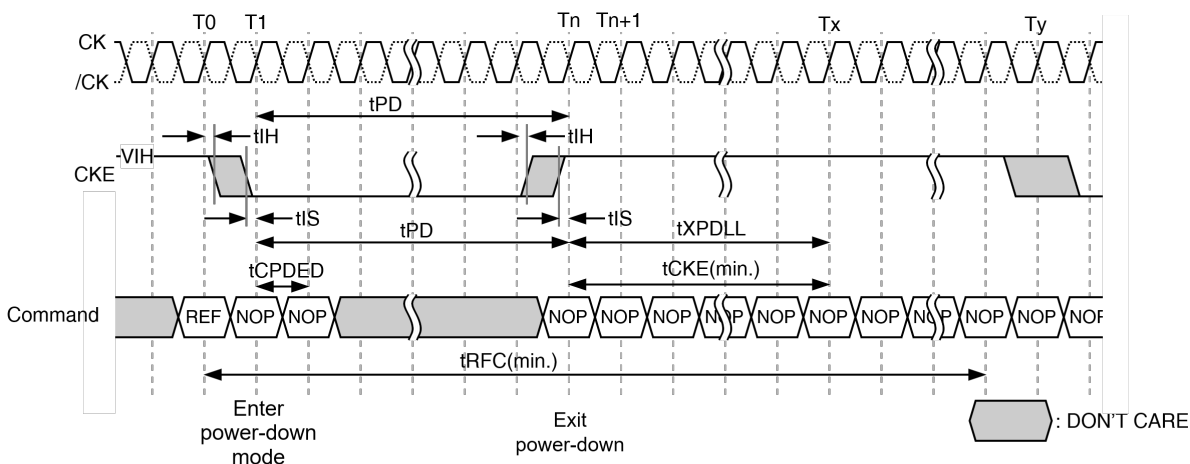
1.  $t_{XP}$  must be satisfied before issuing the command
2.  $t_{XPDLL}$  must be satisfied (referenced to registration of PD exit) before next power-down can be entered.



**Power-Down Entry/Exit Clarifications (2)**

#### Case 3:

If an early PD Entry is issued after Refresh command, once PD Exit is issued, NOP or DESL with CKE high must be issued until  $t_{RFC}$  from the refresh command is satisfied. This means CKE cannot be de-asserted twice within  $t_{RFC}$  window.



Note: \* Synchronous ODT Timing starts at the end of  $t_{XPDLL}$  (min.)

**Power-Down Entry/Exit Clarifications (3)**

#### 9.18.4. Input Clock Frequency Change during Precharge Power-Down

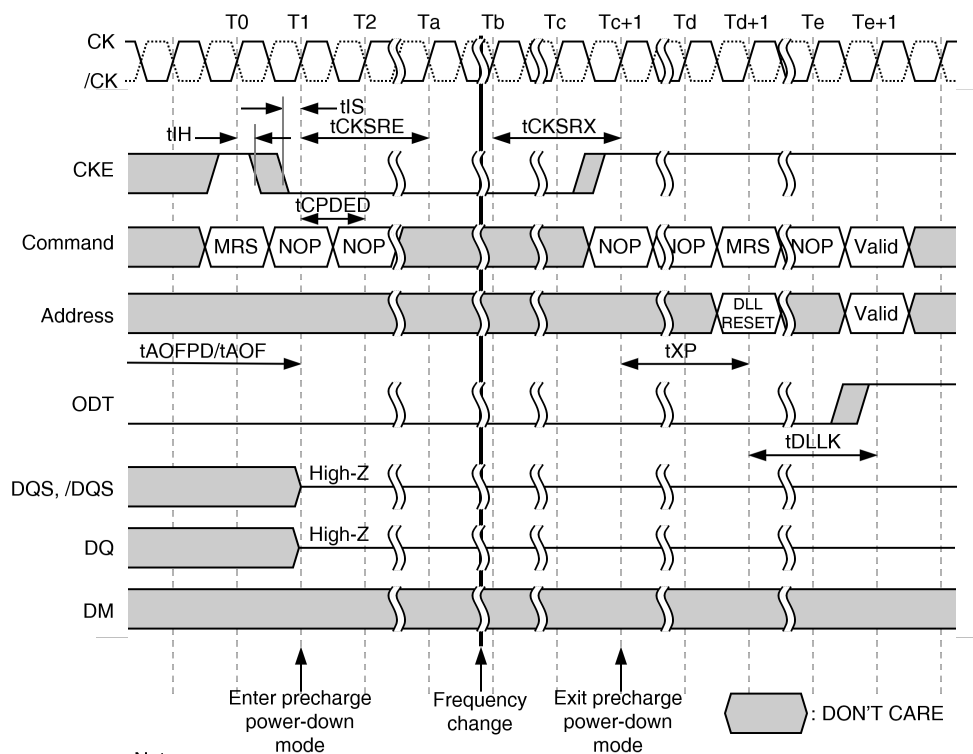
Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (Spread Spectrum Clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) self-refresh mode and (2) precharge power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the self-refresh entry and exit specifications must still be met as outlined in Self-Refresh section.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode.) ODT must be at a logic low ensuring RTT is in an off state prior to entering Precharge Power-down mode and CKE must be at a logic low. A minimum of tCKSRE must occur after CKE goes low before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable low levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL reload period, ODT must remain low. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in the figure Clock Frequency Change in Precharge Power-Down Mode.

#### 9.19. On-Die Termination (ODT)

DT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance



Notes:

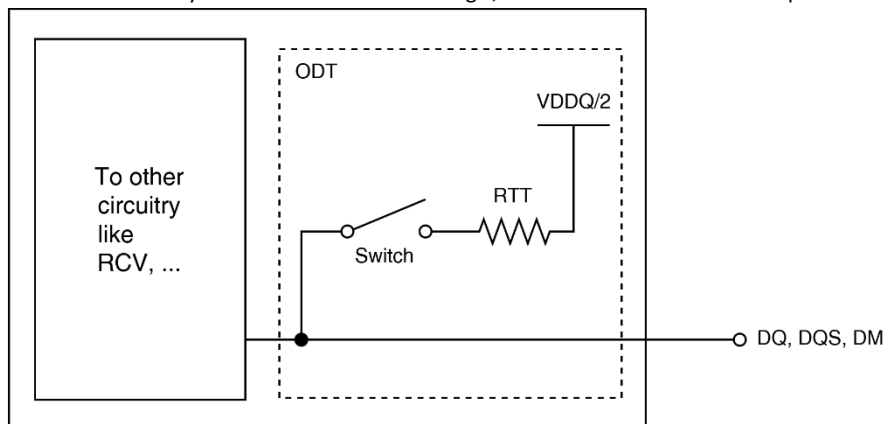
1. Applicable for both slow exit and fast exit precharge power-down.
2. tCKSRE and tCKSRX are self-refresh mode specifications but the values they represent are applicable here.
3. tAOFPD and tAOF must be satisfied and outputs high-z prior to T1; refer to ODT timing for exact requirements.

#### Clock Frequency Change in Precharge Power-Down Mode

for each DQ, DQS, /DQS and DM via the ODT control pin. For  $\times 16$  configuration ODT is applied to each DQU, DQL, DQSU, /DQSU, DQSL, /DQSL, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT feature is turned off and not supported in Self-Refresh mode.  
A simple functional representation of the DRAM ODT feature is shown in figure Functional Representation of ODT.

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control



**Functional Representation of ODT**

information, see below. The value of  $RTT$  is determined by the settings of mode register bits (see MR1 programming figure in the section Programming the Mode Register). The ODT pin will be ignored if the Mode Register MR1 is programmed to disable ODT and in self-refresh mode.

#### 9.19.1. ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 bits A2 or A6 or A9 are non-zero. In this case the value of  $RTT$  is determined by the settings of those bits.

Application: Controller sends WRIT command together with ODT asserted.

- One possible application: The rank that is being written to provide termination.
- DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR)
- DRAM does not use any write or read command decode information
- The Termination Truth Table is shown in the Termination Truth Table

[Termination Truth Table]

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 bits A2, A6 and A9 in general)

### 9.19.2. Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Active mode
- Idle mode with CKE high
- Active power-down mode (regardless of MR0 bit A12)
- Precharge power-down mode if DLL is enabled during precharge power-down by MR0 bit A12.

In synchronous ODT mode, RTT will be turned on or off ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by:  $ODTLon = WL - 2$ ;  $ODTLoff = WL - 2$ .

#### ODT Latency and Posted ODT

In Synchronous ODT mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal.

$ODTLon = CWL + AL - 2$ ;  $ODTLoff = CWL + AL - 2$ . For details, refer to DDR3 SDRAM latency definitions.

[ODT Latency Table]

Parameter	Symbol	Value	Unit
ODT turn-on Latency	ODTLon	$WL - 2 = CWL + AL - 2$	nCK
ODT turn-off Latency	ODTLoff	$WL - 2 = CWL + AL - 2$	nCK

### 9.19.3. Synchronous ODT Timing Parameters

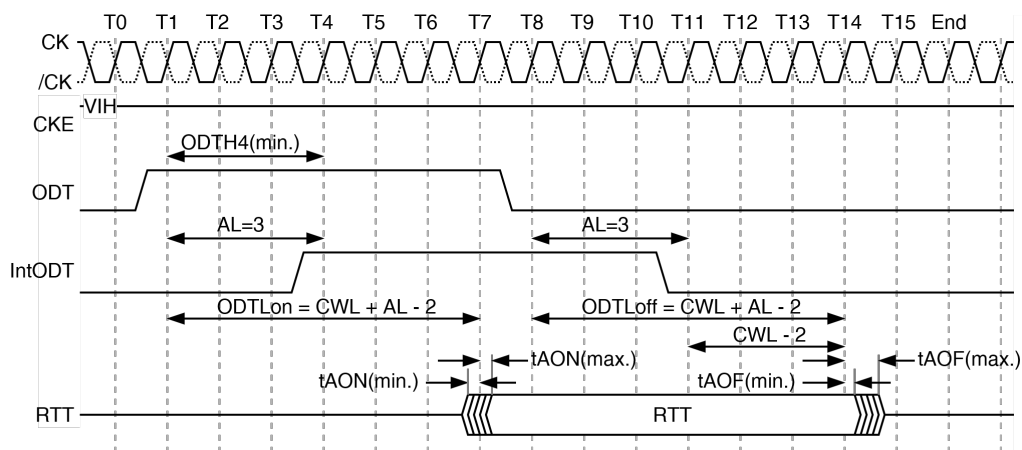
In synchronous ODT mode, the following timing parameters apply (see Synchronous ODT Timing Examples (1)):

ODTLLow, ODTLLOff, tAON, (min.), (max.), tAOF, (min.), (max.) Minimum RTT turn-on time (tAON min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn-on time (tAON max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

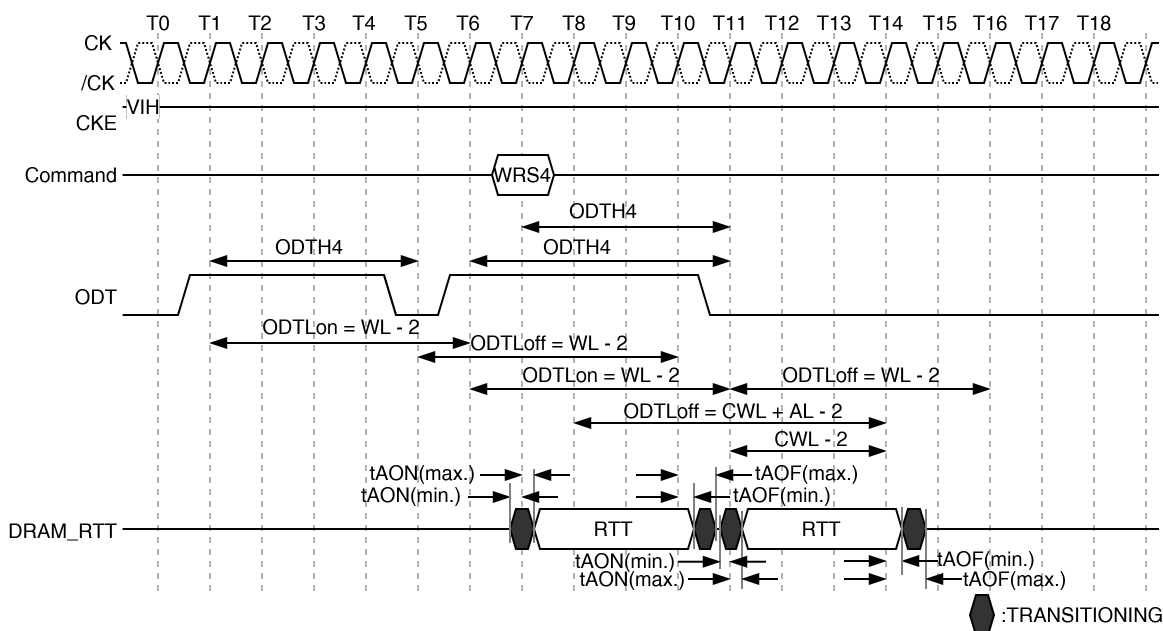
Minimum RTT turn-off time (tAOF min) is the point in time when the device starts to turn-off the ODT resistance.

Maximum RTT turn-off time (tAOF max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTTH4 (BL4) or ODTTH8 (BL8) after the Write command (see figure Synchronous ODT Timing Examples (2)). ODTTH4 and ODTTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.



**Synchronous ODT Timing Examples (1): AL=3, CWL = 5;  
ODTLon = AL + CWL - 2 = 6; ODTLoff = AL + CWL - 2 = 6**



**Synchronous ODT Timing Examples (2)\*: BC4, WL = 7**

ODT must be held high for at least ODT<sub>H4</sub> after assertion (T1); ODT must be kept high ODT<sub>H4</sub> (BC4) or ODT<sub>H8</sub> (BL8) after write command (T7). ODT<sub>H</sub> is measured from ODT first registered high to ODT first registered low, or from ODT registered high at T6 ODT must not go low before T11 as ODT<sub>H4</sub> must also be satisfied from the registration of the write command at T7.

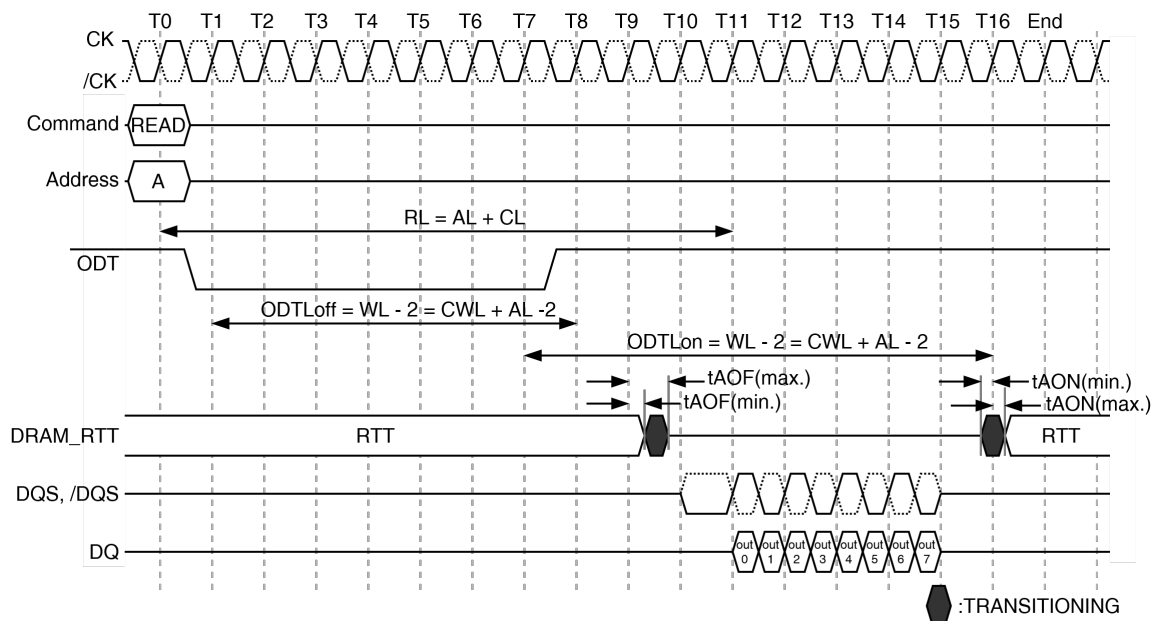
#### 9.19.4. ODT during Reads

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may nominally not be enabled until one clock cycle after the end of the post-amble as shown in the example in the figure below.

Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in the figure below.

ODT must be disabled externally during Reads by driving ODT low.

(example:  $CL = 6$ ;  $AL = CL - 1 = 5$ ;  $RL = AL + CL = 11$ ;  $CWL = 5$ ;  $ODT_{Lon} = CWL + AL - 2 = 8$ ;  $ODT_{Loff} = CWL + AL - 2 = 8$ )



Example of ODT during Reads

#### Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

#### Functional Description:

The Dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to '1'. The function and is described as follows:

- Two RTT values are available: RTT\_Nom and RTT\_WR.
  - The value for RTT\_Nom is pre-selected via bits A[9,6,2] in MR1
  - The value for RTT\_WR is pre-selected via bits A[10,9] in MR2
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength RTT\_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WRIT, WRITA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT\_WR is selected.
  - A latency ODTLcnw8 (for BL8, fixed by MRS or selected OTF) or ODTLcnw4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT\_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table Latencies and Timing Parameters Relevant for Dynamic ODT shows latencies and timing parameters, which are relevant for the on-die termination control in Dynamic ODT mode:

When ODT is asserted, it must remain high until ODT4 is satisfied. If a write command is registered by the SDRAM with ODT high, then ODT must remain high until ODT4 (BC4) or ODT8 (BL8) after the write command (see the figure Synchronous ODT Timing Examples (2)). ODT4 and ODT8 are measured from ODT registered high to ODT registered low or from the registration of a write command until ODT is registered low.

[Latencies and Timing Parameters Relevant for Dynamic ODT]

Parameter	Symbol	Defined from	Defined to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	Registering external ODT signal high	Tuning termination on	ODTLon=WL-2	nCK
ODT turn-off Latency	ODTLoff	Registering external ODT signal low	Tuning termination off	ODTLoff=WL-2	nCK
ODT latency for changing from RTT_Nom to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_Nom to RTT_WR	ODTLcnw=WL-2	nCK
ODT latency for changing from RTT_WR to RTT_Nom (BC4)	ODTLcnw4	Registering external write command	Change RTT strength from RTT_WR to RTT_Nom	ODTLcnw4=4 + ODTLoff	nCK
ODT latency for changing from RTT_WR to RTT_Nom (BL8)	ODTLcnw8	Registering external write command	Change RTT strength from RTT_WR to RTT_Nom	ODTLcnw8=6 + ODTLoff	nCK
Minum ODT high time after ODT assertion	ODTH4	Registering ODT high	ODT registered low	ODTH4(min.)=4	nCK
Minum ODT high time after write (BC4)	ODTH4	Registering write with ODT high	ODT registered low	ODTH4(min.)=4	nCK
Minum ODT high time after write (BL8)	ODTH8	Registering write with ODT high	ODT registered low	ODTH8(min.)=6	nCK
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	0.3 to 0.7	tCK(avg)



### 9.19.5. Mode Register Settings for Dynamic ODT Mode:

The table Mode Register for RTT Selection shows the mode register bits to select RTT\_Nom and RTT\_WR values.

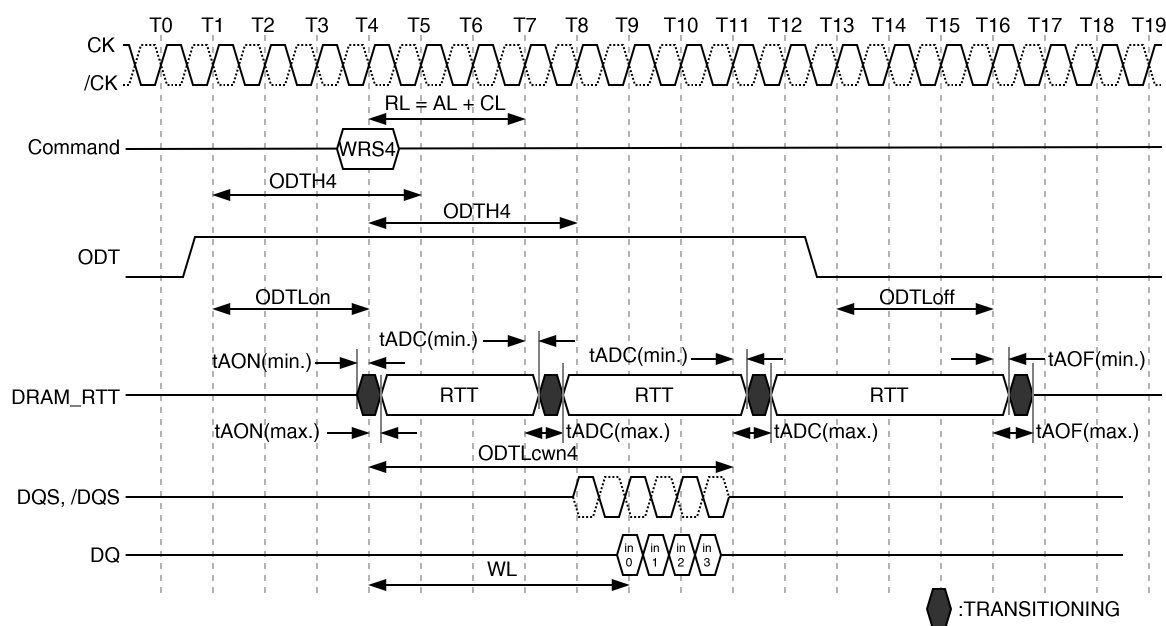
[Mode Register for RTT Selection]

MR1			RTT_Nom (RZQ)	RTT_Nom (Ω)	MR2		RTT_WR (RZQ)	RTT_WR* (Ω)
A9	A6	A2			A10	A9		
0	0	0	off	off	0	0	Dynamic ODT OFF: Write does not affect RTT value	
0	0	1	RZQ/4	60	0	1	RZQ/4	60
0	1	0	RZQ/2	120	1	0	RZQ/2	120
0	1	1	RZQ/6	40	1	1	Reserved	Reserved
1	0	0	RZQ/12* <sup>2</sup>	20	—	—	—	—
1	0	1	RZQ/8* <sup>2</sup>	30	—	—	—	—
1	1	0	Reserved	Reserved	—	—	—	—
1	1	1	Reserved	Reserved	—	—	—	—
					—	—	—	—

Notes: 1. RZQ = 240 $\Omega$ .

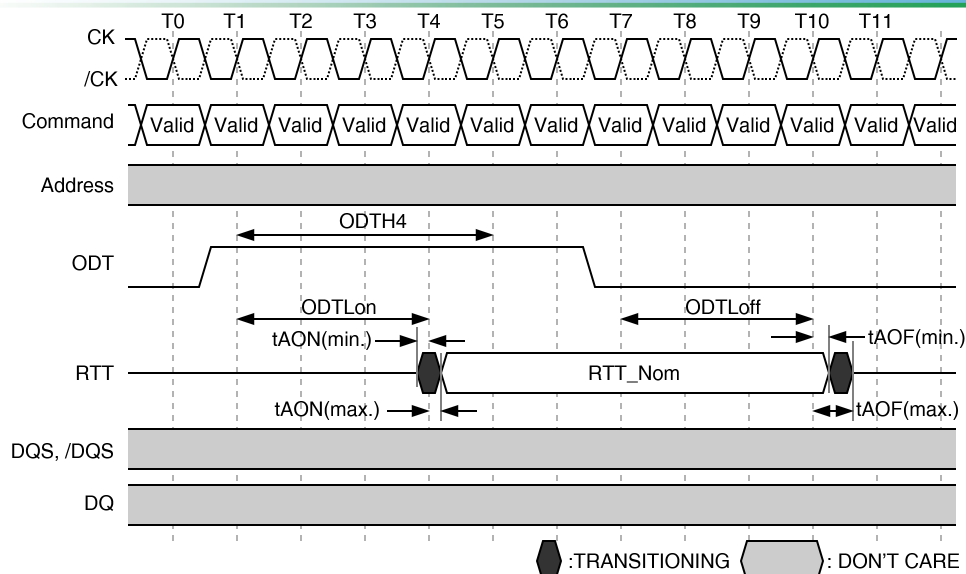
2. If RTT\_Nom is used during WRITES, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

### 9.19.6. ODT Timing Diagrams



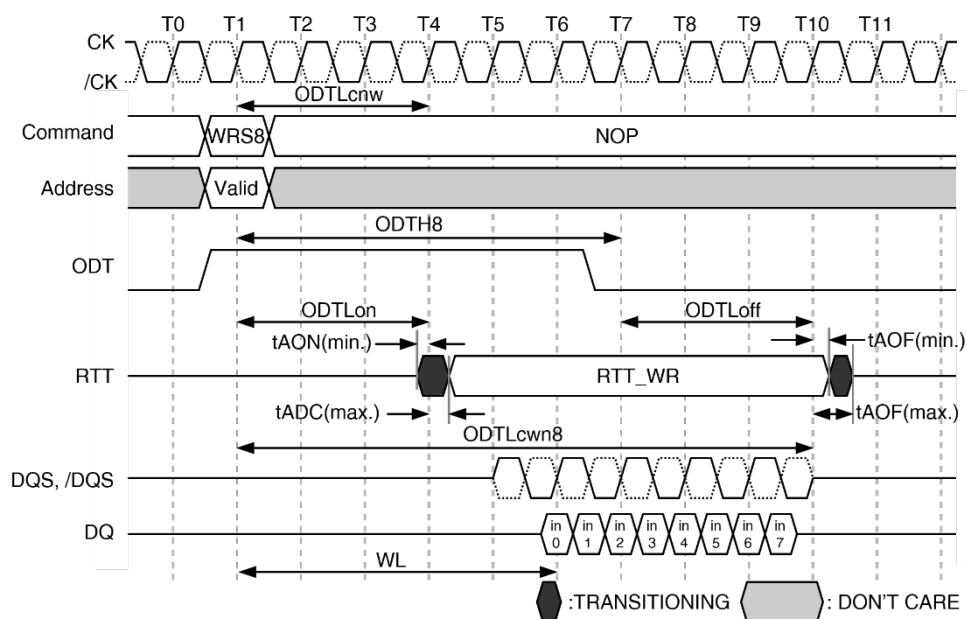
Note: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. ODLH4 applies to first registering ODT high and to the registration of the write command. In this example ODLH4 would be satisfied if ODT is low at T8 (4 clocks after the write command).

### Dynamic ODT: Behavior with ODT Being Asserted Before and after the Write\*



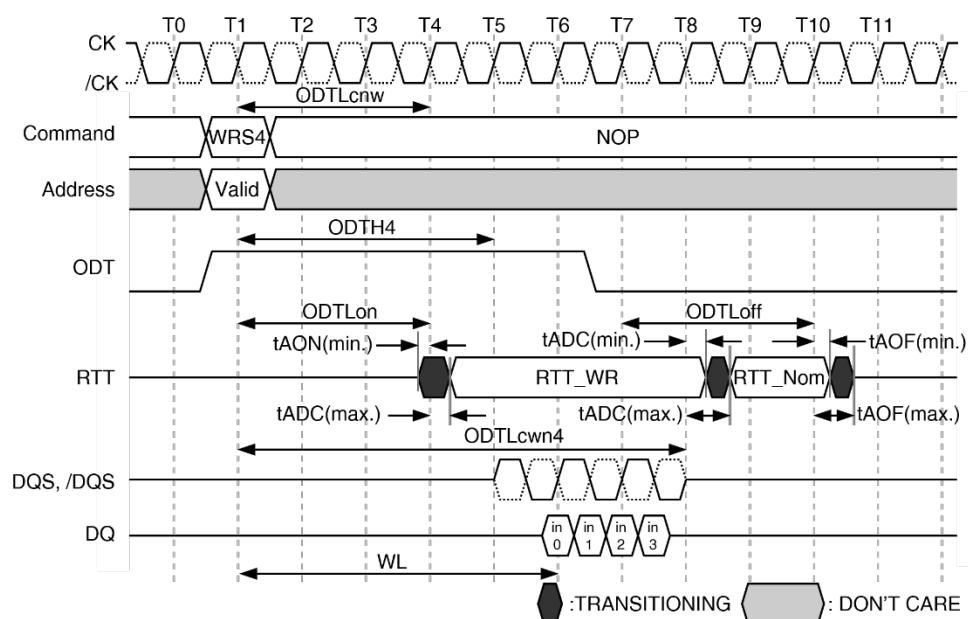
Note: ODT<sub>H4</sub> is defined from ODT registered high to ODT registered low, so in this example ODT<sub>H4</sub> is satisfied; ODT registered low at T5 would also be legal.

#### Dynamic ODT\*: Behavior without Write Command; AL = 0, CWL = 5



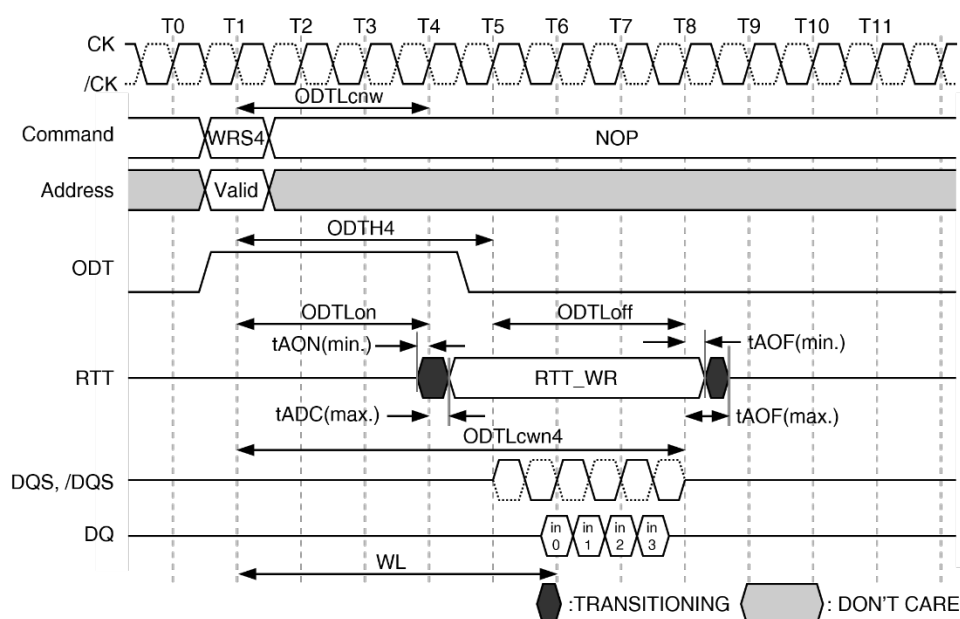
Note: Example for BL8 (via MRS or OTF), AL = 0, CWL = 5. In this example ODT<sub>H8</sub> = 6 is exactly satisfied.

#### Dynamic ODT\*: Behavior with ODT Pin Being Asserted Together with Write Command for Duration of 6 Clock Cycles



Note: ODT4 is defined from ODT registered high to ODT registered low, so in this example ODT4 is satisfied; ODT registered low at T5 would also be legal.

**Dynamic ODT\*: Behavior with ODT Pin Being Asserted Together with Write Command for a Duration of 6 Clock Cycles, Example for BC4 (via MRS or OTF), AL = 0, CWL = 5.**



Note: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. In this example ODT4 = 4 is exactly satisfied.

### Dynamic ODT\*: Behavior with ODT Pin Being Asserted Together with Write Command for Duration of 4 Clock Cycles

### 9.19.7. Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLL-on mode, but DLL is temporarily disabled (i.e., frozen) in precharge power-down (by MR0 bit A12).

Precharge power-down mode if DLL is disabled during precharge power-down by MR0 bit A12.

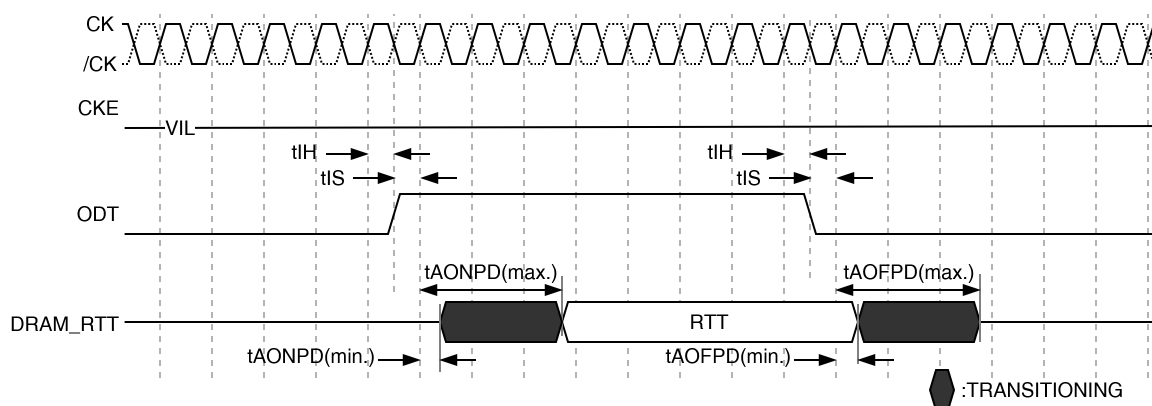
In asynchronous ODT timing mode, internal ODT command is not delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply (see figure Asynchronous ODT Timings): tAONPD (min.), (max.), tAOFPD (min.), (max.)

Minimum RTT turn-on time (tAONPD (min.)) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn-on time (tAONPD (max.)) is the point in time when the ODT resistance is fully on. tAONPD (min.) and tAONPD (max.) are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPD (min.)) is the point in time when the device's termination circuit starts to turn off the ODT resistance. Maximum ODT turn-off time (tAOFPD (max.)) is the point in time when the on-die termination has reached high impedance. tAOFPD (min.) and tAOFPD (max.) are measured from ODT being sampled low.

In precharge power-down, ODT receiver remains active, however no read or write command can be issued, as the



#### Asynchronous ODT Timings on DDR3 SDRAM with Fast ODT Transition: AL is Ignored

respective address/command receivers may be disabled.

[Asynchronous ODT Timing Parameters for All Speed Bins]

Symbol	Parameters	min.	max.	Unit
tAONPD	Asynchronous RTT turn-on delay (power-down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (power-down with DLL frozen)	2	8.5	ns

[ODT for Power-Down (with DLL Frozen) Entry and Exit Transition Period]

Description	min.	max.
tAONPD	$\min \{ \text{ODT}_{\text{Lon}} \times \text{tCK} + \text{tAON}(\text{min.}); \text{tAONPD}(\text{min.}) \}$	$\max \{ \text{ODT}_{\text{Lon}} \times \text{tCK} + \text{tAON}(\text{max.}); \text{tAONPD}(\text{max.}) \}$
	$\min \{ (\text{WL} - 2) \times \text{tCK} + \text{tAON}(\text{min.}); \text{tAONPD}(\text{min.}) \}$	$\max \{ (\text{WL} - 2) \times \text{tCK} + \text{tAON}(\text{max.}); \text{tAONPD}(\text{max.}) \}$
tAOFPD	$\min \{ \text{ODT}_{\text{Loff}} \times \text{tCK} + \text{tAOF}(\text{min.}); \text{tAOFPD}(\text{min.}) \}$	$\max \{ \text{ODT}_{\text{Loff}} \times \text{tCK} + \text{tAOF}(\text{max.}); \text{tAOFPD}(\text{max.}) \}$
	$\min \{ (\text{WL} - 2) \times \text{tCK} + \text{tAOF}(\text{min.}); \text{tAOFPD}(\text{min.}) \}$	$\max \{ (\text{WL} - 2) \times \text{tCK} + \text{tAOF}(\text{max.}); \text{tAOFPD}(\text{max.}) \}$

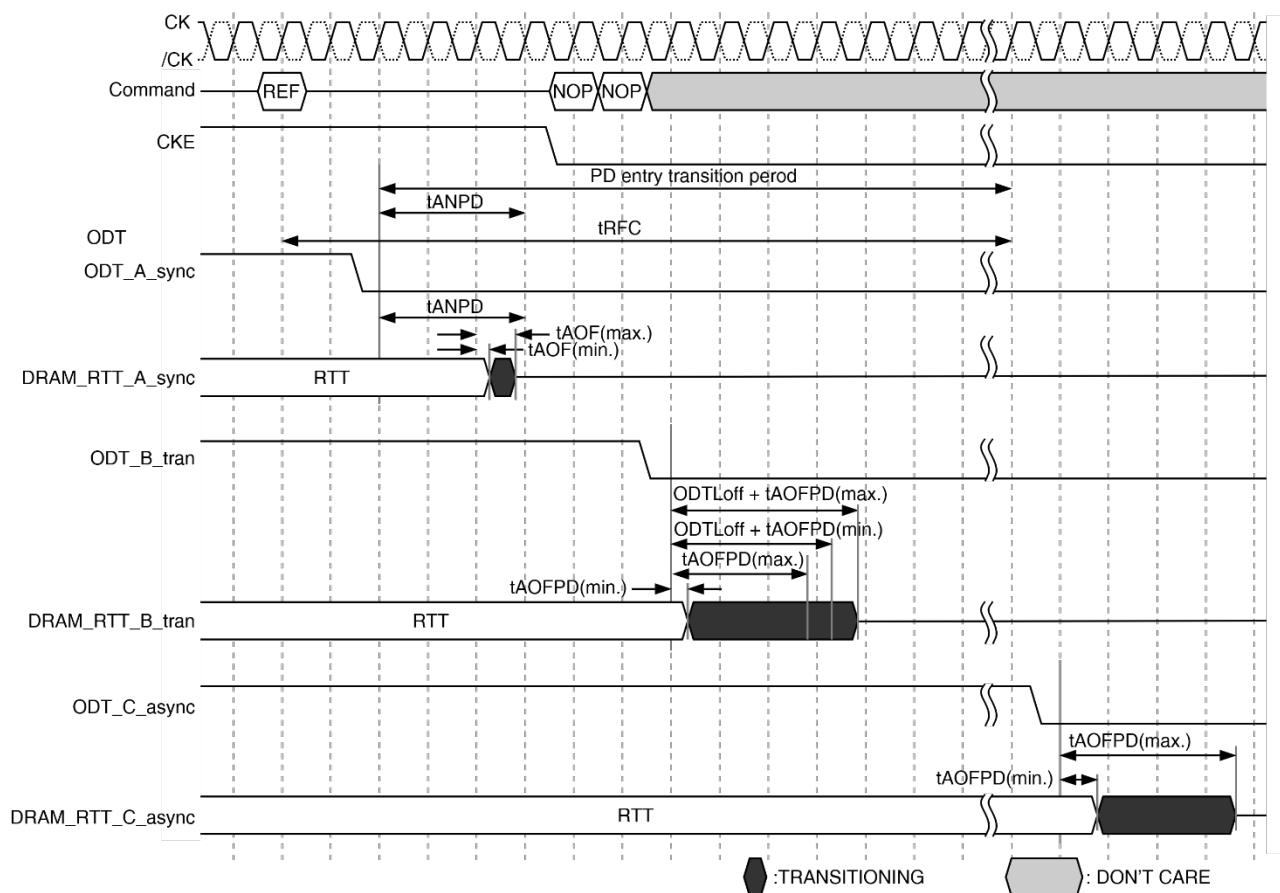
### 9.19.8. Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in precharge power-down mode by the setting of bit A12 in MR0 to 0 there is a transition period around power-down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

This transition period ends when CKE is first registered low and starts tANPD before that. If there is a Refresh command in progress while CKE goes low, then the transition period ends tRFC after the refresh command. tANPD is equal to (WL - 1) and is counted (backwards) from the clock cycle where CKE is first registered low.

ODT assertion during the transition period may result in an RTT change as early as the smaller of  $t_{AONPD}(\min.)$  and  $(ODT_{Lon} \times t_{CK} + t_{AON}(\min.))$  and as late as the larger of  $t_{AONPD}(\max.)$  and  $(ODT_{Lon} \times t_{CK} + t_{AON}(\max.))$ . ODT de-assertion during the transition period may result in an RTT change as early as the smaller of  $t_{AOFPD}(\min.)$  and  $(ODT_{Loff} \times t_{CK} + t_{AOF}(\min.))$  and as late as the larger of  $t_{AOFPD}(\max.)$  and  $(ODT_{Loff} \times t_{CK} + t_{AOF}(\max.))$ . Note that, if AL has a large value, the range where RTT is uncertain becomes quite large.

The figure below shows the three different cases: ODT\_A, synchronous behavior before  $t_{ANPD}$ ; ODT\_B has a state change during the transition period; ODT\_C shows a state change after the transition period.



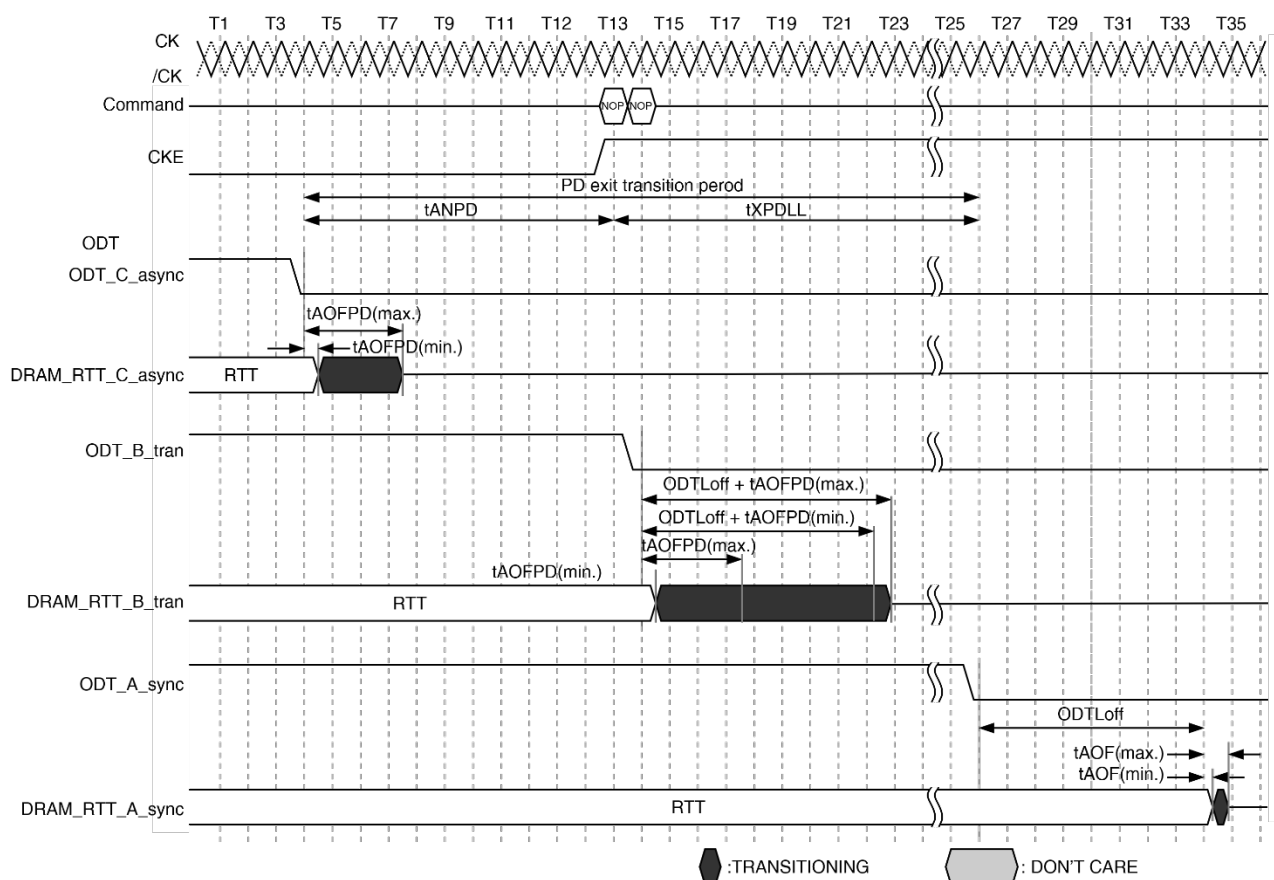
**Synchronous to Asynchronous Transition During Precharge Power-Down**  
(with DLL Frozen) Entry (AL = 0; CWL = 5;  $t_{ANPD} = WL - 1 = 4$ )

### 9.19.9. Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in precharge power-down mode by the setting of bit A12 in MR0 to 0, there is also a transition period around power-down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts  $t_{ANPD}$  before CKE is first registered high, and ends  $t_{XPDLL}$  after CKE is first registered high.  $t_{ANPD}$  is equal to  $(WL - 1)$  and is counted backward from the clock cycle where CKE is first registered high. ODT assertion during the transition period may result in an RTT change as early as the smaller of  $t_{AONPD}(\min.)$  and  $(ODT_{Lon} \times t_{CK} + t_{AON}(\min.))$  and as late as the larger of  $t_{AONPD}(\max.)$  and  $(ODT_{Lon} \times t_{CK} + t_{AON}(\max.))$ . ODT de-assertion during the transition period may result in an RTT change as early as the smaller of  $t_{AOFPD}(\min.)$  and  $(ODT_{Loff} \times t_{CK} + t_{AOF}(\min.))$  and as late as the larger of  $t_{AOFPD}(\max.)$  and  $(ODT_{Loff} \times t_{CK} + t_{AOF}(\max.))$ . See ODT for Power-Down (with DLL Frozen) Entry and Exit Transition Period table.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. The figure below shows the three different cases: ODT\_C, asynchronous response before  $t_{ANPD}$ ; ODT\_B has a state change of ODT during the transition period; ODT\_A shows a state change of ODT after the transition period with synchronous response.



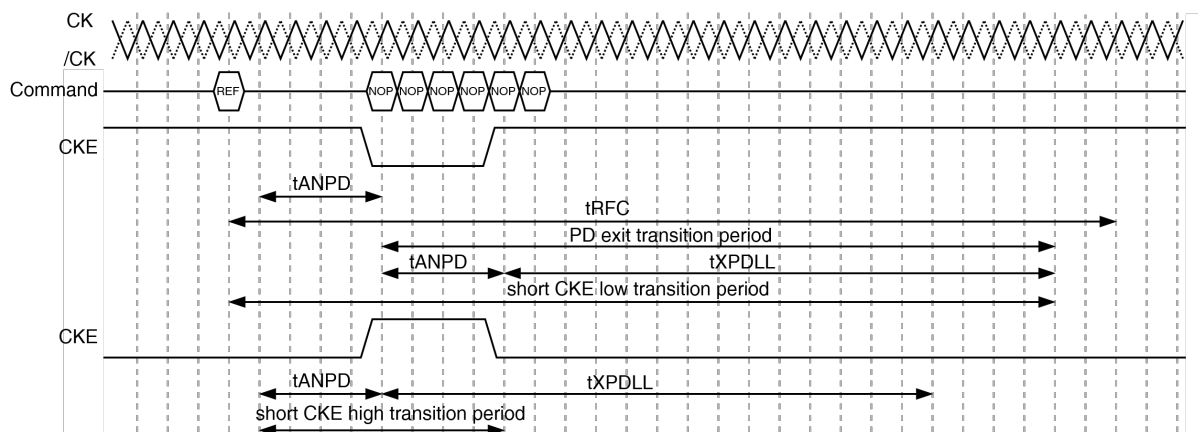
**Asynchronous to Synchronous Transition during Precharge Power-Down (with DLL Frozen) Exit**  
(CL = 6; AL = CL - 1; CWL = 5;  $t_{ANPD} = WL - 1 = 9$ )

#### 9.19.10. Asynchronous to Synchronous ODT Mode during Short CKE high and Short CKE Low Periods

If the total time in precharge power-down state or idle state is very short, the transition periods for power-down entry and power-down exit may overlap. In this case the response of the DDR3 SDRAM RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the power-down entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in idle state is very short, the transition periods for power-down exit and power-down entry may overlap. In this case the response of the DDR3 SDRAM RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the power-down exit transition period to the end of the power-down entry transition period.

Note that in the bottom part of figure below it is assumed that there was no refresh command in progress when idle state was entered.



**Transition Period for Short CKE Cycles with Entry and Exit Period Overlapping**  
(AL = 0, WL = 5, tANPD = WL - 1 = 4)

## 9.20. ZQ Calibration

ZQ calibration command is used to calibrate DRAM RON and ODT values. DDR3 SDRAM needs longer time to calibrate RON and ODT at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calibrated values are transferred from calibration engine to DRAM I/O which gets reflected as updated RON and ODT values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQ correction}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

where TSens = max (dRTTdT, dRONdTM) and VSens = max (dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5%/°C, VSens = 0.15%/mV, Tdriftrate = 1°C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as:

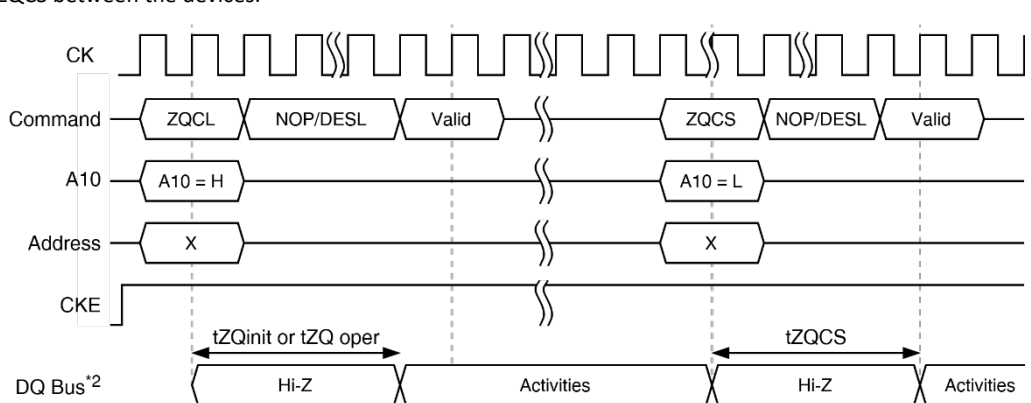
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper or tZQCS. The quiet time on the DRAM channel allows in accurate calibration of RON and ODT. Once DRAM calibration is achieved the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self-refresh. Upon self-refresh exit, DDR3 SDRAM will not perform an I/O calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self-refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit or tZQCS between the devices.



Note:

1. CKE must be continuously registered high during the calibration procedure.
2. ODT must be disabled via ODT signal or MRS during calibration procedure.
3. All device connected to DQ bus should be High impedance during calibration.

### ZQ Calibration

#### 9.20.1. ZQ External Resistor Value and Tolerance

DDR3 SDRAM has a 240Ω ±1% tolerance external resistor connecting from the DDR3 SDRAM ZQ pin to ground. The resistor can be used as single DRAM per resistor.



Change History			
Document name: DSA3T4GF340CBFF.(Rev.#)			
Rev. #	Who	When	What
01	SAE	2022-12-12	Initial version derived from DSA3T4GF2340CBFP.06; Removed x4 Part number and related information from Specifications, Features, Ordering Information, Package Ball Assignment, Block Diagram and Address Pins Table; Updated Output capacitance of /DED pin in Pin Capacitance

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